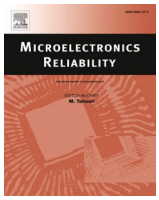
Microelectronics Reliability 155 (2024) 115372

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Review paper

Research progress of hybrid bonding technology for three-dimensional integration

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ARTICLE INFO

Keywords:
Hybrid bonding
Three-dimensional packaging
Materials
Equipment
Process

ABSTRACT

Computing power based artificial intelligence will profoundly change the productivity and production relations, and the integrated circuit industry begin to rely on three-dimensional (3D) integration to increase the computing power. The traditional liquid phase welding interconnection can not reconcile the huge difference between devices size and package pitch. Hybrid bonding is a new type of interconnection, through the simultaneous bonding of dielectric layer and metal layer, the interconnection density can be improved by orders of magnitude. In this paper, the research progress of hybrid bonding for 3D integration has been reviewed in detail from the perspectives of materials, equipment and processes. By analyzing the bonding characteristics of metal and dielectric materials, comparing the performance of bonding modules and platforms, detailing the processes of each bonding step, it provides a comprehensive overview and comparison of different research achievements in recent years. In the future, it is urgent to develop the materials, equipment and processes of hybrid bonding collaboratively, which will support the 3D packaging to the aim of small distance, high density and low power consumption.

1. Introduction

With the rapid development of artificial intelligence, high-performance computing, and the Internet of Things, the semiconductor industry is approaching the limits of Moore's Law. Increasing the number of transistors and enhancing device functionality by reducing feature sizes on a two-dimensional (2D) plane is becoming increasingly challenging, leading to a post-Moore era. It aims to break through the limitations of Moore's Law [1] by the high-density interconnect in the back-end process. Advanced packaging technology includes chiplet technology [2,3], fan-out packaging [4,5], embedded multi-die interconnect bridge (EMIB) [6,7], and three-dimensional (3D) packaging [8–10]. 3D integrated interconnection offers shorter interconnect paths and higher interconnect density, significantly reducing device size and weight. 3D integration is a key technology in the post-Moore era to support the miniaturization, multifunctionality, and high reliability of semiconductor devices.

Hybrid bonding, as a leading technology in high-density interconnects for 3D stacking, has attracted widespread attention. Hybrid bonding is defined as a permanent bonding technique that combines a dielectric bond with embedded metal to form interconnections between different components, such as wafers or dies [11]. Hybrid bonding technology sidesteps the limitations of traditional scaling by avoiding the use of microbumps, which are challenging to scale down past 10 μm pitches, and instead utilizes small copper-to-copper connections. For hybrid bonding, both the diffusion bonding of metal and the covalent bonding of dielectric realize a stable, robust, and bump-less permanent bonding interface. The unique bonding approach has reduced the pitch and increased the interconnect density, reaching up to 100,000/mm^2. Compared to traditional micro-bump soldering, hybrid bonding offers the following advantages: ultra-high interconnect density, increased bandwidth, lower power consumption, high reliability and high flexibility. Fig. 1 [12–15] illustrates a comparison between hybrid bonding and traditional copper pillar bump technology across multiple performance, such as interconnect pitch, bandwidth, energy efficiency, and performance. Compared to copper pillar, hybrid bonding offers greater bandwidth, higher energy efficiency, and smaller interconnect pitch. This results shows the potential value for the hybrid bonding in 3D

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https://doi.org/10.1016/j.microrel.2024.115372
Received 16 January 2024; Received in revised form 14 March 2024; Accepted 15 March 2024
Available online 23 March 2024

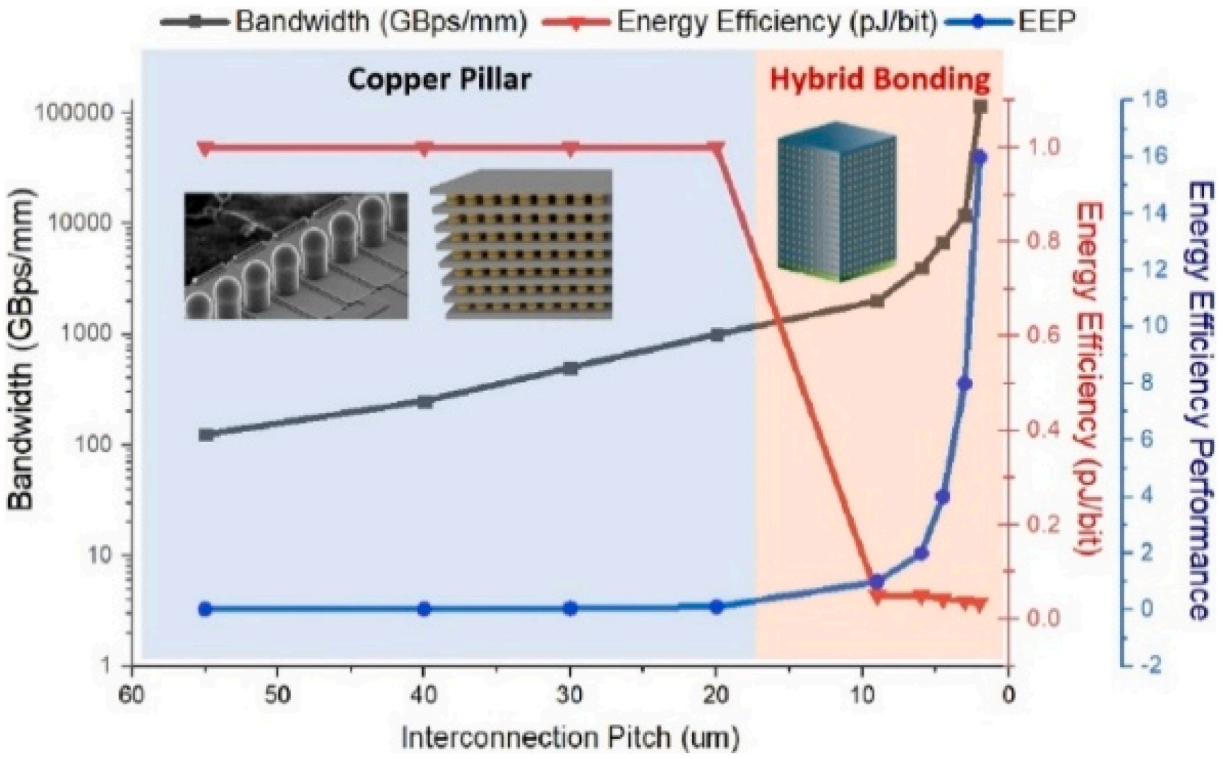


Fig. 1. Comparison Between Copper Pillar Bump Technology and Hybrid Bonding Technology [12–15].

integration.

Hybrid bonding has become known across the industry as direct bond interconnect (DBI). Initially, the Rensselaer Polytechnic Institute (RPI) established and pioneered the development and application of hybrid bonding techniques [16]. RPI has pioneered an approach aimed at solving the future bottleneck of copper/low k interconnects and enabling multifunctional system integration. This early work laid the foundation for further exploration and optimization of this technology. The term "hybrid bonding" itself was first introduced by Interuniversity Microelectronics Centre (IMEC), an international research and development organization that played a crucial role in formulating concepts and advancing this technique. IMEC has made significant contributions to advancing hybrid bonding technologies, particularly in the development of 3D system-on-chip (SoC) architectures [17]. Their research typically focuses on improving semiconductor device performance through innovative packaging and interconnect strategies. IMEC's research in the field of hybrid bonded materials is extremely representative, including not only the TEOS dielectric research, but especially in the field of SiCN hybrid bonding process and bonding temperature regulation [18]. IMEC also made representative studies on the optimization of Die-to-Wafer hybrid bonding process, such as the temporary bonding process, which realized the transfer sequence of die assisted by laser and carried out ultra-low stress collective bonding at room temperature [19]. IMEC's influential role helped to define the method's parameters and its potential applications within the semiconductor industry, particularly in 3D integration and advanced packaging solutions. International Business Machines Corporation (IBM) also made significant contributions to the field of hybrid bonding through extensive experiments and research aimed at improving reliability, scalability, and performance of these connections [20]. In 2006, IBM proposed the possibility of Cu bonding in 3D IC bonding [21]. In 2008 and 2009, the hybrid Cu/adhesive bonding structure was proposed [22,23]. It lays a foundation for the development of hybrid bonding. K.-N. Chen et al. from IBM proposed that the hybrid bonding of cupric oxides showed excellent bonding quality and performance in terms of orientation, bonding strength and environmental osmosis oxidation [24,25]. The excellent performance of the initial reliability and quality evaluation of the cupric oxide hybrid bonding were key milestones in the manufacturability of the hybrid bonding 3D integration technology. Moreover, Samsung has made outstanding achievements in the field of die-to-wafer (D2W) hybrid bonding, and has achieved a D2W process with a bonding strength of 2.5 J/m^2, comparable to the breaking strength of silicon [26]. Samsung's research in the hybrid bonded 3D memory stack package realized the D2W multilayer structure, combined with chemical mechanical polishing (CMP) and plasma activation, and assessed the chip surface quality according to oxide morphology, Cu dishing height, surface hydrophilicity, hydroxyl density and adhesion. The resulting bonded chip has excellent electrical and thermal properties, which is of great significance for the development of 3D packaging [27]. Their work pushed the boundaries of what could be achieved with this technology in terms of device density and interconnect efficiency. These foundational efforts from RPI, IMEC, IBM, Samsung, other companies and institutes have paved the way for hybrid bonding to become a cornerstone of modern semiconductor device fabrication and packaging, enabling higher performance and more compact integrated circuits.

Hybrid bonding can be classified as wafer-to-wafer (W2W) and die-to-wafer (D2W) bonding. W2W involves the direct bonding of two wafers, whereas D2W refers to the bonding of multiple known good dies onto the bottom wafer. Hybrid bonding, as an emerging packaging technology, combines metal and dielectric materials through the bonding process, which promotes new demand on bonding materials, especially dielectric materials. From the perspective of equipment, hybrid bonding relies on the integrated equipment with high control precision, high reliability, and functional integration. Prominent equipment manufacturers are actively developing hybrid bonding equipment to facilitate the breakthroughs and applications in this field. Moreover, the process flow of hybrid bonding encompasses several stages, including chemical mechanical polishing (CMP), cleaning, dicing, activation, pre-bonding, and annealing. The process requires strict particle control, and the quality of metal-dielectric hybrid bonding is collectively influenced by each step. Therefore, this paper aims to review the recent research on advanced packaging technology using

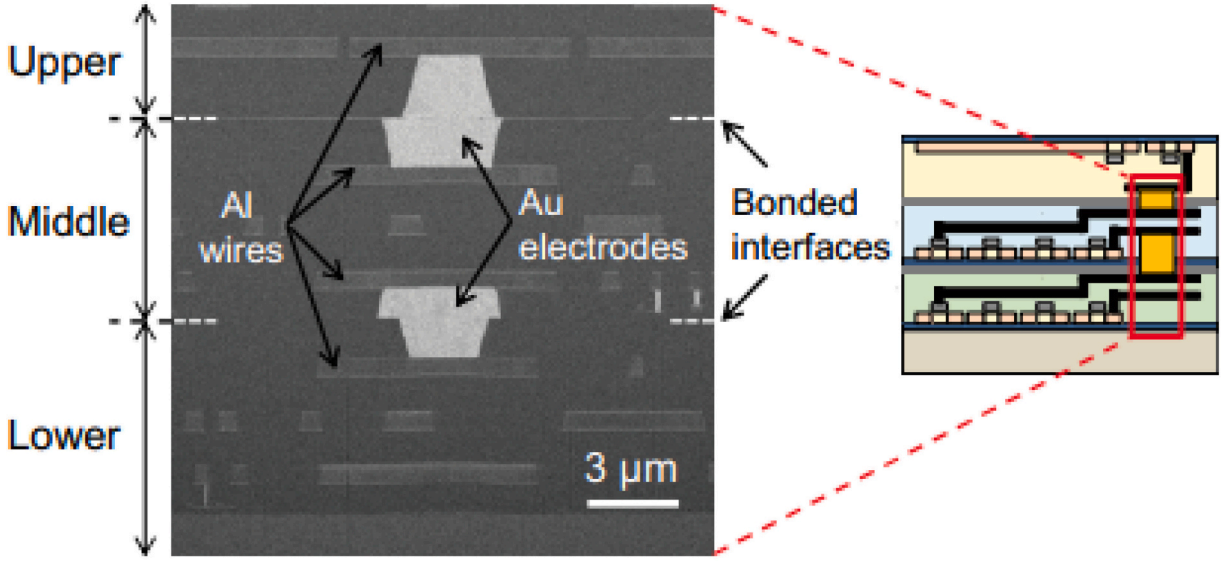


Fig. 2. SEM cross-section image of three-layer stacked pixel sensor - gold electrodes and aluminum leads [29]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

hybrid bonding, focusing on materials, equipment, and processes. It will analyze the current challenges and forecast the development trends, providing new insights into 3D integration.

2. Hybrid bonding: Metal and dielectric materials

The wafer surface in hybrid bonding consists of two materials: metal and dielectric. Metal materials are characterized by their superior electrical and thermal conductivities, which are essential for efficient signal and heat transfer. Dielectric materials demonstrate strong insulation properties, playing a crucial role in maintaining electrical integrity. During the hybrid bonding process, the upper wafer/die are aligned with the lower wafer based on the metal and dielectric areas, and the bonds between metal-to-metal and dielectric-to-dielectric are subsequently formed. There are three distinct bonding interfaces: metal-to-metal, dielectric-to-dielectric, and metal-to- dielectric.

In hybrid bonding 3D packaging, metal materials are necessary to form vertical electrical interconnects between chip and wafer through metal-to-metal diffusion bonding. The metal material exhibits outstanding electrical conductivity and thermal conductivity, enabling efficient signal propagation and heat transfer. The effective heat dissipation is increasingly important to mitigate thermal buildup at interconnect nodes as interconnect density escalates [28]. Commonly used metals in bonding include copper, aluminum, gold, and silver [29,30]. Copper, a popular metal material in hybrid bonding, stands out with an electrical resistivity of 1.72 μΩ·cm and a thermal conductivity of 401 W (m^{-1} K^{-1}), rendering the high electrical and thermal conductivity. The widespread application of copper in hybrid bonding packaging can be attributed to its low resistance and superior dissipating heat properties. Consequently, copper has become the predominant metal interconnect material in integrated circuits. However, its coefficient of thermal expansion (CTE) is 16.5 × 10^{-6} K^{-1}, significantly higher than that of dielectric material. This high CTE may cause thermal stress at the interface during the annealing stage of hybrid bonding. Aluminum is a popular choice for packaging materials due to its lightweight nature, cost-effectiveness, and ease of processing. However, its high coefficient of thermal expansion (23.2 × 10^{-6} K^{-1}) can result in significant thermal stress during device operation, which may lead to failures and limit its widespread use. Gold and silver are preferred for conductive connections in specific demanding packaging applications, such as microelectronic connectors, high-frequency, and high-power devices, due to their excellent electrical conductivity, despite their higher costs.

In the selection of metal materials, it is necessary to consider factors including electrical conductivity, thermal conductivity, corrosion resistance, mechanical strength and cost to fulfill the demands of specific applications. Hybrid bonding packaging is a multifaceted process, entailing not only the selection of apt metal materials but also the assessment of interface characteristics and compatibility between metals and dielectrics to guarantee robust bonding and reliable packaging performance.

Masahide Goto et al. have investigated a pixel-level interconnect hybrid bonding stacking technology for image sensors with SiO_2 dielectric and Au metal layers [29]. Fig. 2 displays a nanoscale silicon layer at the bonding interface enables effective diffusion of Au atoms, thereby establishing efficient electrical contacts between Au electrodes. This advancement, utilizing SOI wafers with Au/SiO_2 hybrid bonding, led to the development of a three-layer stacking technology with pixel-level interconnects, showcasing improved mechanical strength of the stacked wafers. Post-bonding Energy Dispersive X-Ray Spectroscopy (EDX) analysis at the interface confirmed encapsulation of Au within the thin Si layer, which fosters robust electrical contacts between the Au electrodes and augments the mechanical integrity of the stacked chips. This innovative approach not only underscores its merits in improving electrical contact performance, but also paves new way for the advanced integration and optimization of image sensors.

Copper, a predominant metal material used in hybrid bonding, has diverse characteristics as highlighted by Yun Zhang et al., who noted that “not all copper is the same” in the context of hybrid bonding processes [31]. The grain size of electroplated copper significantly impacts the effectiveness of bonding across the interface. By adjusting the electroplating process with specific additives enabled the formation of nanostructured copper characterized by high symmetry and exceptional room-temperature stability. The preferred ⟨111⟩ crystal orientation of the copper is particularly beneficial for facilitating copper-to-copper diffusion bonding in hybrid bonding. This research underscores that, beyond mere metal composition, the granular structure and crystalline orientation within the solder pads are pivotal in determining the outcomes of hybrid bonding processes.

Furthering this exploration, Kai-Cheng Shie et al. from Taiwan combined nano-twinned Cu (nt-Cu) with low-temperature dielectrics to realize the low-temperature hybrid bonding [32]. Their innovative copper-first approach altered the conventional sequence of dielectric

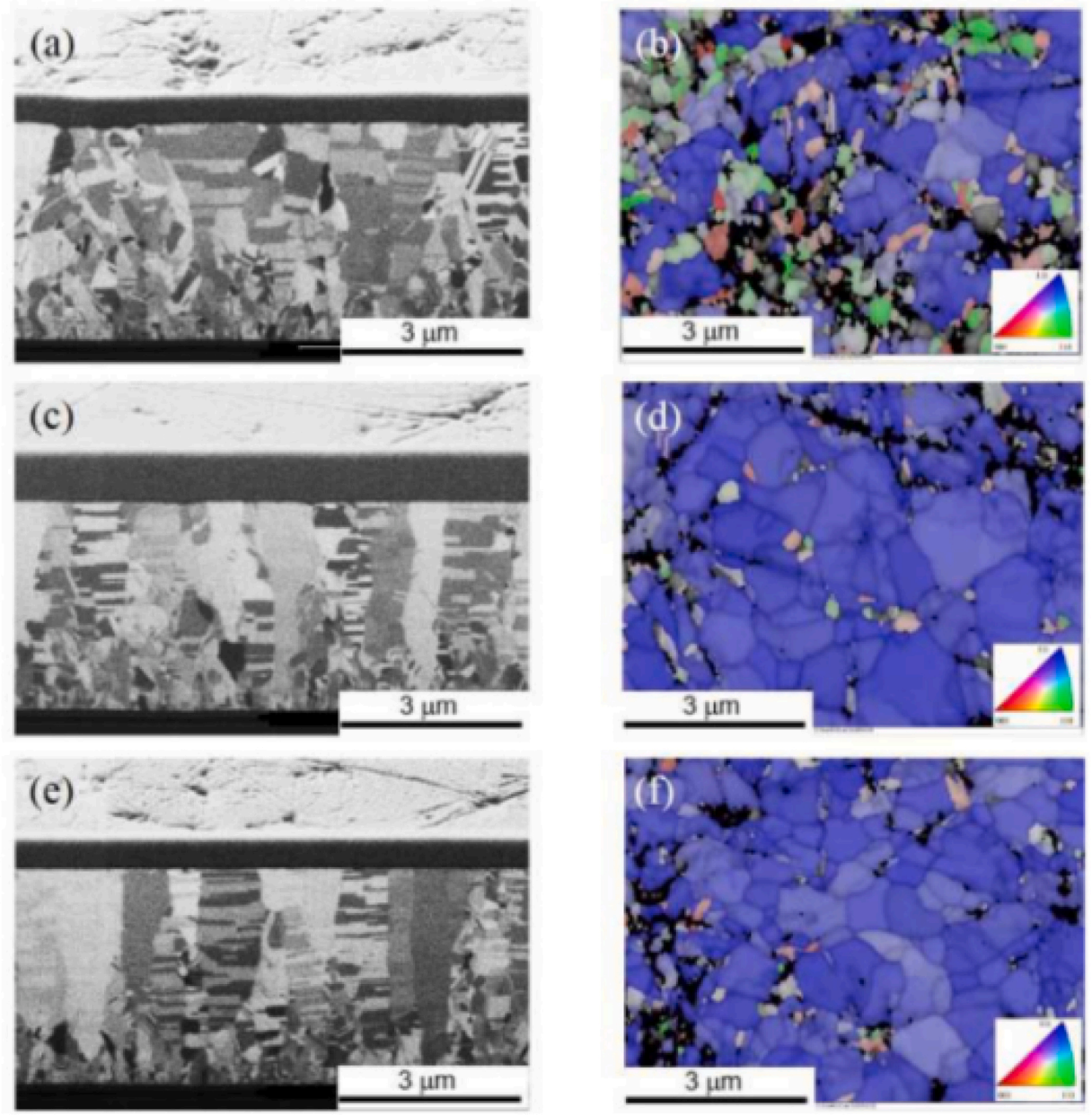


Fig. 3. Top view of FIB cross section and EBSD image at different electroplating current densities. (a)(b) 1 ASD; (c)(d) 2 ASD; (e)(f) 3 ASD [33].

coating and copper plating, resulting in the preparation of surfaces with a dominant (111) orientation in nt-Cu. This methodology entailed initially electroplating patterned nt-Cu, followed by integrating dielectrics in both pre- and post-CMP stages. They successfully carried out two distinct hybrid bonding processes, employing low-temperature polyimide (PI) and non-conductive paste (NCP), effectively instituting a Cu + NCP hybrid bonding method conducive to a minimized thermal budget.

Furthermore, Chih-Cheng Hsiao and colleagues embarked on a thorough investigation of wafer-level nano-twinned copper (nt-Cu) for direct bonding applications [33]. The process involved adjusting the electroplating current density (A/dm^2, ASD), thereby attaining a high percentage of (111) surface orientation, reaching up to 97 % as evidenced in Fig. 3. Focused Ion Beam (FIB) and Electron Backscatter Diffraction (EBSD) verified the dimensional and orientational attributes of the columnar grains. The nt-Cu demonstrated an extremely fined surface roughness of 0.72 nm after CMP. Remarkably, nt-Cu direct bonding accomplished after 1 h at 250 °C without significant bonding voids. The bonding integrity among BCB layers at the same temperature was notably robust, and there was no delamination in the bonding interface, with an average shear strength exceeding 24 MPa.

Chih Chen et al. conducted further research on the utilization of nanotwin layers in hybrid bonding, wherein they fabricated a fine-spacing hybrid bond by employing thick PECVD SiO_2 as the dielectric layer and highly oriented nanotwin Cu as the metal layer on a 12-in. silicon wafer. In this study, the hybrid bonding temperature of Cu/SiO_2 was reduced to 200 °C, resulting in a bonding strength exceeding 30 MPa [34].

Numerous studies have demonstrated that metal passivation can effectively lower the bonding temperature and enhance the quality of bonds formed during mixed bonding processes [35–41]. Kuan-Neng Chen et al. proposed depositing a 10 nm Ti layer as a passivating agent on the Cu surface in a hybrid bonding structure to prevent internal Cu oxidation and lower the bonding temperature to 180 °C [35]. Subsequently, Pd was applied as metal passivator to achieve 150 °C bonding temperature with contact resistance of 10^{-7} Ω·cm^2 [36]. Recently,

Table 1
Comparison of metal passivation bonding methods [35–41].

Types of metals	Bonding temperature(°C)	Contact resistance ($\Omega \cdot cm^2$)	Bonding shear strength (MPa)
Silver nanolayers [38]	180	/	6.5
Ti passivation [35]	180	7×10^{-4}	/
Pd passivation [36]	150	2×10^{-7}	7.03
Au passivation [37]	120	1×10^{-7}	2.65
Cr/Au [39]	70	3×10^{-7}	7.3
Cluster Ag passivation [40]	70	/	21.95
Ti/Au [41]	40	/	7

Kuan-Neng Chen et al. proposed a Cr/Au and Ti/Au passivation schemes to reduce the bonding temperature to room temperature [39,40]. The comparison of different metal passivation methods is listed in Table 1.

Dielectric materials play a crucial role in isolating water and oxygen from the environment to prevent the metal corrosion, which also providing mechanical support and electrical isolation. Dielectric materials can be categorized into two groups: organic and inorganic materials [42]. Organic dielectrics mainly consist of polymers like benzocyclobutene (BCB) and polyimide (PI), while inorganic dielectrics consist mostly of silicon-based materials such as silicon dioxide, silicon nitride, and SiCN. A notable characteristic of polymer dielectrics is their tendency to slide during the bonding or curing phases, potentially leading to misalignment of the bond structure and a consequent reduction in bond strength. Conversely, silicon-based inorganic dielectrics have commendable insulating properties and do not require curing, which are well-suited for the Damascene process. This makes them essential dielectrics for hybrid bonding application.

Chenxi Wang et al. from Harbin Institute of Technology have developed a VUV/O_3 activated direct bonding method for achieving the integration of SiC on Si and SiO_2 substrates [43]. Following VUV/O treatment, surface hydrophilicity was achieved, as evidenced by an increase in the hydroxyl group observed in the Raman spectrum. The UV-VIS transmission spectrum of the SiC/glass pair exhibited excellent optical visibility. Additionally, they investigated the use of O_2 plasma activation as a pre-treatment to bond hydrophilic surfaces at room temperature and devised a stepped annealing curve to reduce the bonding temperature to 200 °C while ensuring strong bonds and achieving a uniform and defect-free bonding interface [44].

Masaya Kawano et al. conducted on a comprehensive study of dielectric materials in hybrid bonding [18]. They meticulously analyzed and compared various attributes of these materials, including morphology and roughness pre- and post-Chemical Mechanical Polishing (CMP), as well as the resulting bonding strength (refer to Table 2). The results showed a descending order of bonding strength among dielectrics: polymers > SiCN > TEOS SiO_2 > SiN. Importantly, the bonding strength of polymers exceeded 2.5 J/m^2, with a shear strength over 50 MPa. The relatively lower Young's modulus of polymers helps mitigate the tensile stresses associated with copper diffusion during annealing, thus reducing the risk of dielectric layer detachment. Nevertheless, the tendency of polymers to accumulate fine scratches during CMP presents an unresolved challenge. On the other hand, SiCN demonstrated exceptionally low roughness and minimal copper recess after CMP. Its favorable hydrophilicity contributes to high bonding strength, establishing it as a premium dielectric material for hybrid bonding processes.

Interuniversity Microelectronics Centre (IMEC) has proposed using of a new PECVD SiCN layer in the hybrid bonding process. The SiCN deposited at175°C can achieve a void-free hybrid bonding interface and a high bonding strength even at low temperature (200 °C) [45]. In this study, four different SiCN materials with varying ratios of Si, C, N, and H were deposited by PECVD at temperatures lower than 200 °C. Scanning Acoustic Microscopy (SAM) was utilized to detect porosity. The surface roughness of the SiCN layer after deposition and CMP were measured respectively using Atomic Force Microscopy (AFM). It revealed that the Young's modulus of the dielectric film increased with the deposition temperature. The porosity decreased with increasing temperature, and the bonding energy increased with the post-bonding annealing temperature. The CSAM results in Fig. 4 indicate that the voids vary in different SiCN films, with SiCN A exhibiting the largest voids in the center position.

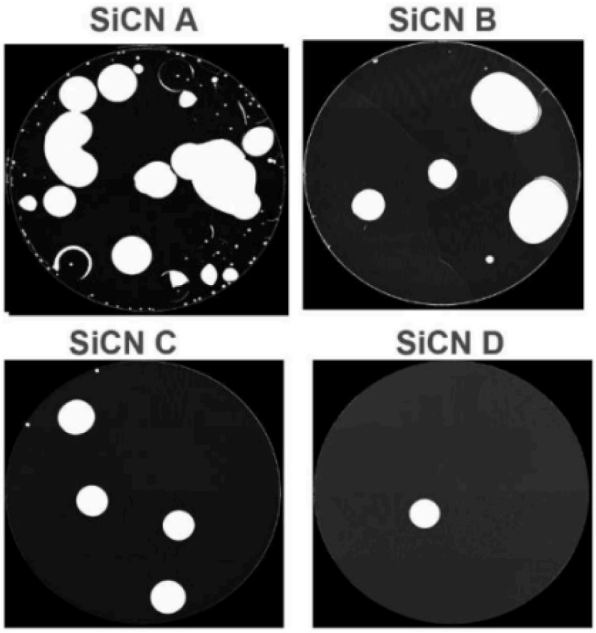
Satoshi Yoneda's research team has successfully developed a novel dielectric material known as polyimide-based photosensitive adhesive (PI). This material is designed specifically for the low-temperature hybrid bonding below 250 °C. [46]. It shows great potential as a permanent dielectric for hybrid bonding, with superior step absorption capacities compared to typical inorganic dielectrics. Table 3 presents a comparative analysis of the new PI, indicating a lower glass transition temperature (Tg) compared to the standard PI1. However, its thermal decomposition temperature (T_{d1}) exceeds the typical temperature range for copper annealing. The new PI shows a dielectric constant comparable to traditional PI1 and a lower dissipation factor at a frequency close to the 5 GHz frequency used by logic integrated circuits. Following pre-bonding and thermal compression bonding (TCB), the novel PI material exhibits an outstanding bonding performance, with a shear strength exceeding 23 MPa. Significantly, under external stress, the bonding failure mode shifts from common interface delamination to the silicon substrate. This shift emphasizes the exceptional bonding properties of the novel PI, marking a notable advancement in the field of dielectric materials for hybrid bonding.

The research group simultaneously investigated a hybrid bonding technique utilizing copper (Cu) and polyimide (PI) [46]. This study involved optimizing the application of aqueous acids, accurately controlling the extent of Cu protrusion, and determining appropriate conditions for both temporary and permanent bonding. The empirical data showed that using citric or ascorbic acid solutions, while maintaining the Cu protrusion height at 80 nm, substantially improved the bonding effectiveness of Cu electrodes. The study identified the optimal parameters for achieving permanent bonding, specifically a temperature of 250 °C and a pressure of 5 MPa. These variables were crucial in enhancing the Cu and PI hybrid bonding procedures.

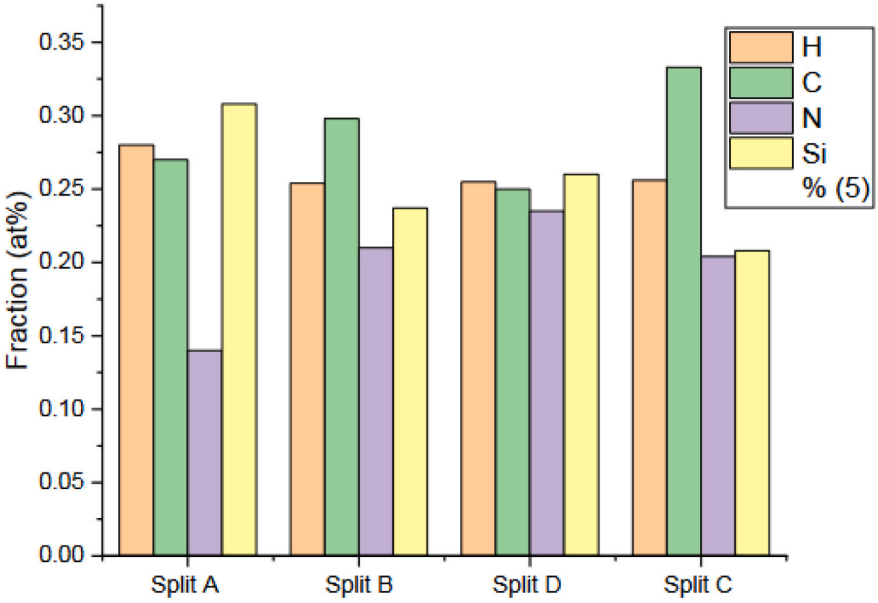
Suga's research group at the University of Tokyo suggested an inventive method of integrating a nanolayer of iron (Fe) or other metals into the dielectric layer used for bonding [47]. This method involves the

Table 2
Comparison of surface properties and bonding strength of mixed bonding medium materials [18].

Dielectric code	Average contact angle (°)	Surface roughness Ra (nm)		Bond strength	
		Before CMP	After CMP	Bonding energy(J/m^2)	Shear strength (MPa)
Low temperature TEOS SiO_2	11	0.6–0.8	0.3–0.4	0.9–1.1	12–15
High temperature TEOS SiO_2	9	0.6–0.8	0.3–0.4	1.2–1.4	18–20
SiN	15	1.1–1.25	0.6–0.75	0.6–0.8	7–10
SiCN (high-carbon)	5	0.45–0.6	0.2–0.3	1.6–1.8	26–30
High temperature polymer	≥45	28–32	1.5–2	>2.5	45–50
Low temperature polymer	23	1.9–2.2	1–1.2	>2.5	35–40



(a) SAM images of SiCN films' bonding



(b) SiCN film element composition

Fig. 4. SiCN film bonded SAM image and element composition [45].

incorporation of either thin layers or clusters of Fe, utilizing their characteristics to decrease the surface polarity of ionic materials. Consequently, this method can shield the surface polarity of ionic materials, effectively neutralizing or shielding undesirable factors or mismatches that may exist between the materials, thus ensuring the tightness and stability of the bond. The application of this technique has demonstrated potential in attaining bond energies comparable to the breaking strength of silicon, which is around 2.5 J/m^2. This novel idea introduces new possibilities in hybrid bonding technology, which could enhance the performance and dependability of bonded interfaces in microelectronic applications (Fig. 5).

3. Hybrid bonding equipment

Hybrid bonding, recognized as an advanced packaging technology, is rapidly progressing towards improved precision and higher density. Strong bonding between dielectric and metal layers requires close control of the wafer warpage, planarity, cleanliness, and alignment accuracy. This necessitates equipment that is precise, efficient and reliable. Leading equipment manufacturers worldwide are investing substantial resources in advanced hybrid bonding equipment research and production to facilitate its widespread adoption. Developed nations have initially emerged as leaders in the wafer bonding equipment industry. Although the Wafer-to-Wafer (W2W) hybrid bonding apparatus has become well-established, the Die-to-Wafer (D2W) hybrid bonding

Table 3
Comparison of performance parameters between new PI and Conventional PI [46].

Curing temperature (°C)	New PI			Conventional PI1	Conventional PI2
	320/1 h	350/1 h	375/2 h	375/1 h	200/2 h
Tensile strength (MPa)	209	175	194	190	190
Elongation (%)	73	79	94	50	41
Young's modulus (GPa)	2.5	2.5	2.5	3.0	3.4
Tg(°C)	232	234	267	290	225
CTE (ppm/K)	99	97	53	50	63
Td_1(°C)	–	–	382	365	277
Dielectric constant at 5GHz	–	–	3.4	3.5	–
Loss factor at 5GHz	–	–	0.0076	0.0148	–

technology is still in the early stages of global study. The complete and advanced solution that combines both wafer-to-wafer (W2W) and die-to-wafer (D2W) hybrid bonding remains elusive, both domestically and globally.

Notable businesses in this field include EV Group (EVG) from Austria and SUSS MicroTec from Germany, renowned for their extensive expertise and longstanding history of technological advancement in wafer bonding equipment development. Their wide range of products is utilized in various fields, such as semiconductors, optoelectronics, and MEMS. Currently, these companies are advancing the development of specialized equipment for hybrid bonding. The future appears promising due to the increased investments from manufacturers, advancements in bonding techniques, and extensive fundamental research. These factors are expected to expedite the development of hybrid bonding equipment. This development is anticipated to make a substantial contribution to the worldwide increase in the utilization of wafer bonding equipment.

SUSS MicroTec, a German company established in 1949, entered the semiconductor equipment industry in the late 1980s. It introduced the initial wafer bonding equipment in 1992. The company's present lineup comprises a range of wafer bonding machines, classified into fully automated and manual models. The manual models require manual intervention for wafer alignment and bonding, which can be challenging to maintain clean and is susceptible to operational errors. In contrast, the fully automatic models are purpose-built for high-precision hybrid bonding applications, such as XBS200, XBS300, and XBC300 models. The XBS200 is specifically engineered for W2W hybrid bonding of 4-in. and 8-in. wafers. The XBS300, succeeding the XBS200, now provides compatibility with 12-in. wafers. The XBC300 is a highly adaptable machine developed in collaboration with Smart Equipment Technology (SET) NEO HB die bonding module. It has the capability to handle both 8-in. and 12-in. wafers for W2W and D2W hybrid bonding, representing the pinnacle of current hybrid bonding technology.

The SUSS MicroTec XBC300 hybrid bonding platform incorporates a cleaning module, activation module, alignment module, wafer bonding module, D2W bonding module, and measurement module. The platform enables the performance of both D2W and W2W hybrid bonding techniques, guaranteeing the cleanliness of the entire process. The cleaning module is compatible with deionized water, citric acid, and SC1 cleaning conditions, and is equipped with megasonic functionality. The activation module uses gases like N_2, O_2, or Ar plasma to activate the surfaces of wafers or dies, enhancing their wettability and surface conditions.

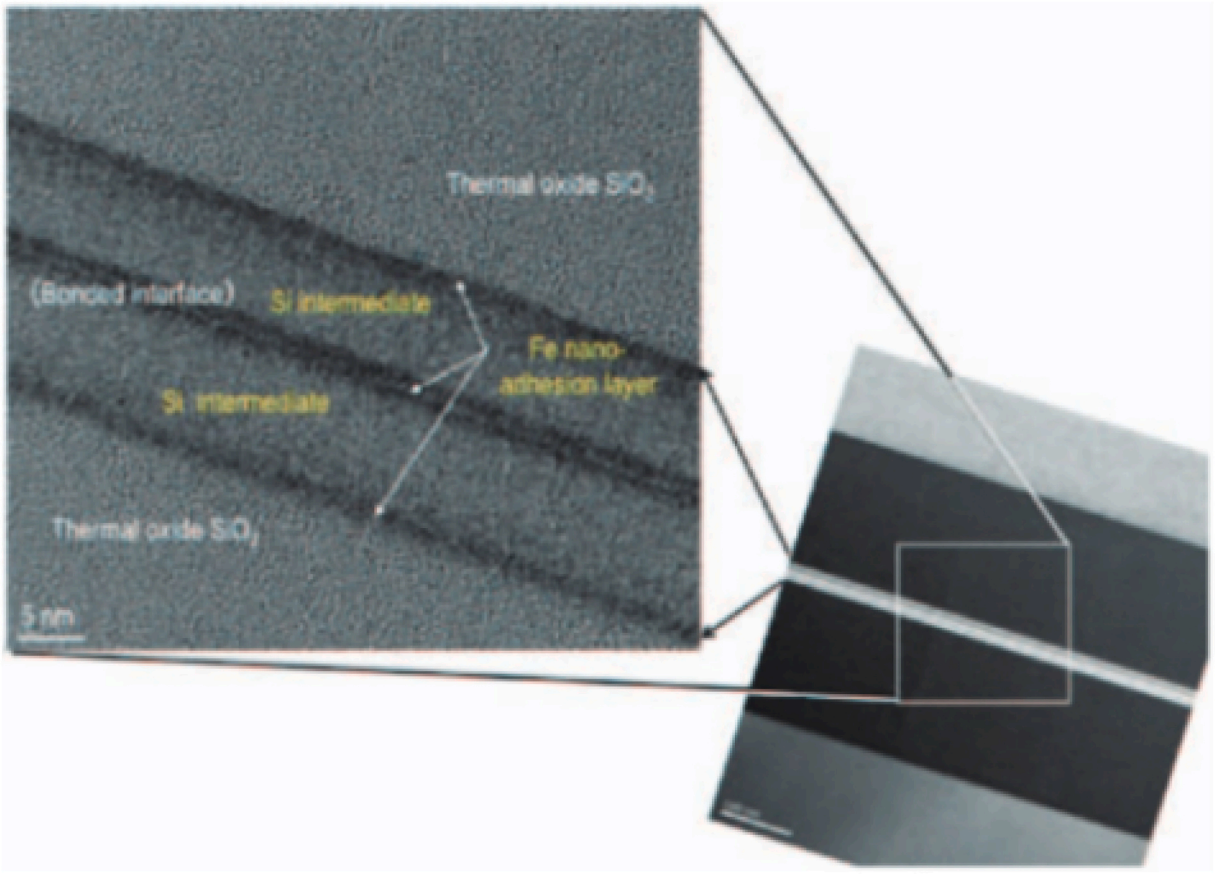


Fig. 5. Insert iron nanolayer bond and interface SAB image [47].

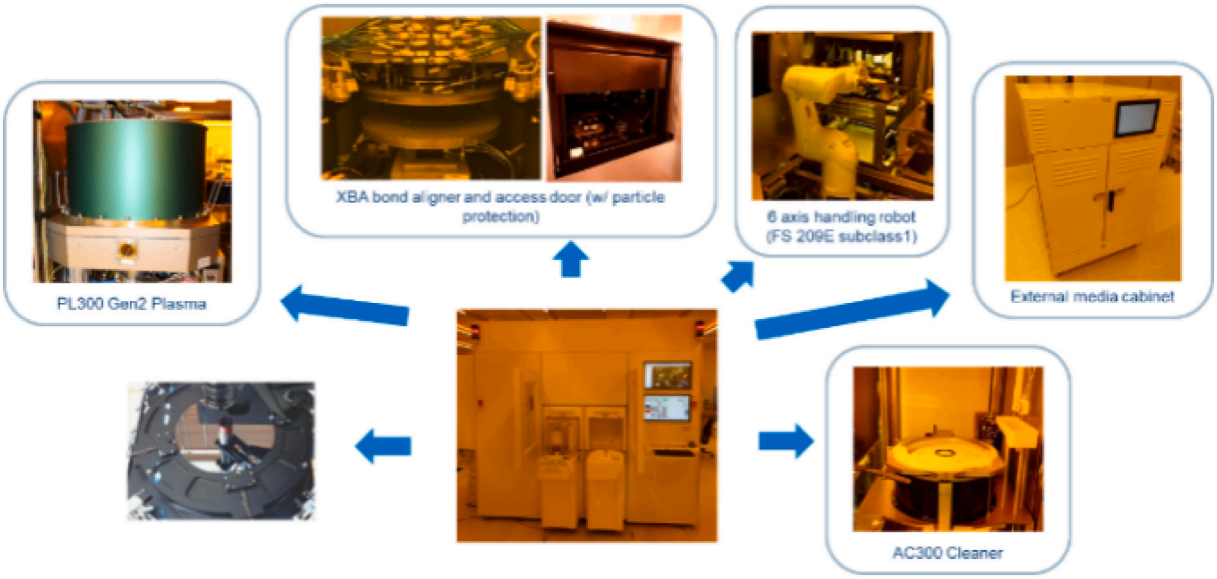


Fig. 6. XBS300 Hybrid bonding platform and modules.

The alignment module now achieves a sub-100 nm alignment precision for W2W hybrid bonding. The D2W bonding module offers continuous pick-and-place bonding procedures, with alignment accuracy of <200 nm. After alignment, the samples are placed into the wafer bonding module, which is capable of accommodating bonding conditions of up to 250 °C and 15kN. The measurement module employs infrared light to detect the overlay and void defects after the bonding process, and subsequently feedbacks the offset to the alignment module for correction (Fig. 6).

Smart Equipment Technology (SET), ASM AMICRA, and Besi are currently leading the D2W hybrid bonding machine industry. The Neo HB equipment manufactured by SET is widely recognized for its outstanding bonding accuracy of ±0.3 μm 3σ. This equipment excels in performing both die bonding and flip-chip bonding processes. It maintains a high level of cleanliness, meeting the ISO 3 standard, and has a throughput capacity of 400 to 800 units per hour (uph). ASM AMICRA's NANO Die Bonder/Flip Chip Bonder offers a bonding accuracy of ±0.3 μm 3σ, equivalent to the precision of Besi's ChameoUltra plus equipment. The alignment accuracy is further improved to ±0.2 μm 3σ.

SUSS and SET, ASM AMICRA and EVG, Applied Materials (AM) and Besi are collaboratly developing the D2W hybrid bonding equipment, respectively. EVG, founded in Austria in 1980, initially focused on research and development in the field of vacuum technology. The EVG Gemini FB is an advanced platform primarily designed for high-performance material hybrid bonding. This system incorporates multiple functional modules, such as cleaning, activation, alignment, bonding, and SmartView NT inspection. The system provides exceptional alignment accuracy, with a precision of <100 nm, and a high throughput ranging from 1000 to 1600 units per hour. Unlike the integrated machine developed by SUSS-SET, EVG's wafer bonding and ASM's D2W bonding modules operate autonomously. Leading manufacturers SUSS, EVG, and AM are actively working on developing integrated solutions for both W2W and D2W hybrid bonding. Their objective is to improve the alignment and bonding accuracy while ensuring rigorous process cleanliness.

Apart from the most essential bonding modules, the equipment for chemical mechanical polishing (CMP), wafer thinning, dicing, and annealing are necessary for the whole hybrid bonding process. Chemical mechanical polishing (CMP), a critical step in hybrid bonding, primarily aims to achieve wafer surface uniformity before the bonding process. Leading CMP machines from AM in the United States and Huahai Qingke in China, dominate the market. These machines are designed to handle a wide range of materials, encompassing dielectrics such as silicon, silicon dioxide, and silicon nitride, as well as metals like copper, tungsten, and aluminum. Successful bonding relies heavily on the flatness and shape of the surface after CMP.

Wafer thinning machines and dicing machines are crucial in the D2W hybrid bonding process, since they are responsible for producing chips with the required dimensions and thickness. DISCO, a prominent Japanese manufacturer, specializes in a wide range of cutting and thinning technologies, such as mechanical dicing, laser dicing, stealth dicing, and plasma dicing. The notable feature of "Dicing before Grind (DBG)" technique involves initially partially cutting the wafer, then subsequently grinding the backside to achieve complete separation of the chips. Stealth Dicing before Grind (SDBG) is an improved version of DBG that utilizes stealth dicing (SD) technology for cutting materials. This method effectively reduces mechanical stress and edge defects that may occur during cutting and thinning processes. As a result, it improves the quality of bonding and the long-term durability of the materials.

After pre-bonding, it is crucial to perform annealing at high temperatures for a long duration in order to promote the diffusion bonding of metals and enhance the bond strength of the dielectric layer. The annealed samples, particularly in W2W layouts, can be heated in standard ovens without worries about misalignment. However, in cases involving chip and wafer bonding in D2W processes, where the bond is not very strong and consists of multiple layers, the annealing process requires meticulous temperature control and cleanliness. To achieve successful D2W hybrid bonding, it is crucial to have annealing equipment that has high precision and precise control over particles. Additionally, the use of mass-production annealing apparatus can greatly enhance the efficiency of the process by annealing pre-bonded wafers together.

The progress in hybrid bonding technology is closely linked to the capabilities and complexity of the related equipment. Achieving higher density, smaller size, and improved performance in packaging technologies requires constant improvement and development of equipment capabilities. Furthermore, as the hybrid bonding processes undergo enhancements and advancements, new demands are naturally imposed on the equipment. This continuous interaction ensures that equipment development remains adaptable and responsive to the evolving demands of sophisticated packaging technologies. The relationship between equipment capabilities and process requirements is mutually beneficial, as each drives the progress of the other. Essentially, the equipment utilized in hybrid bonding is indispensable for the overall effectiveness

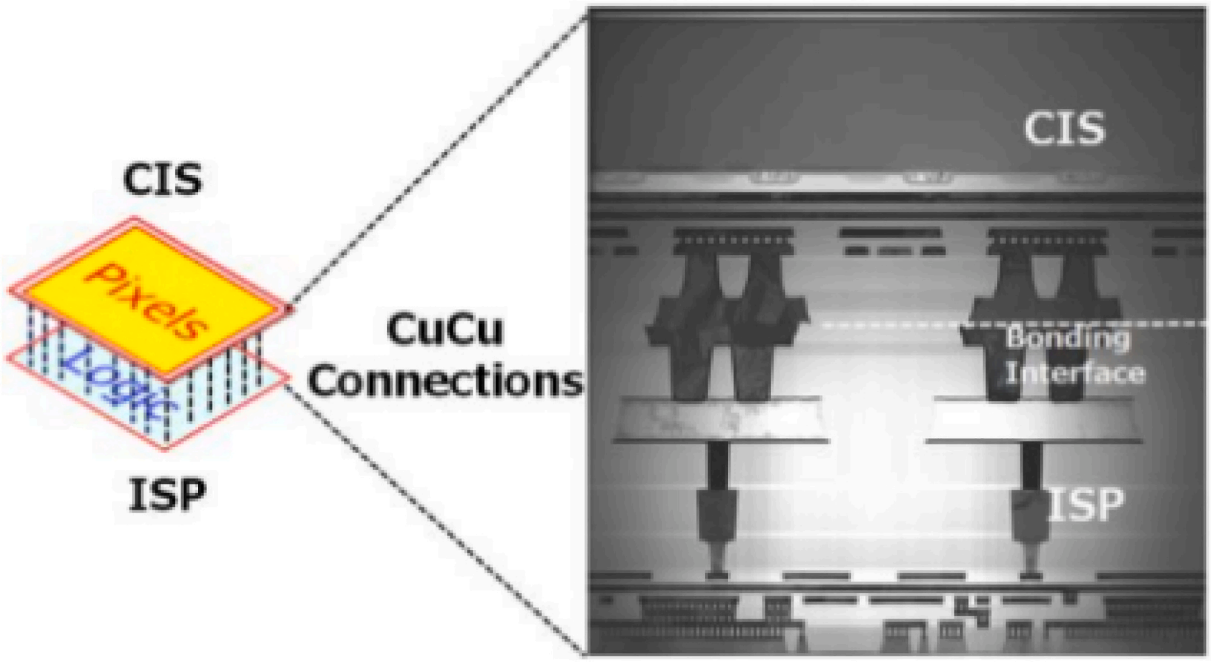


Fig. 7. Image sensor structure diagram of Sony Hybrid bonding technology [49].

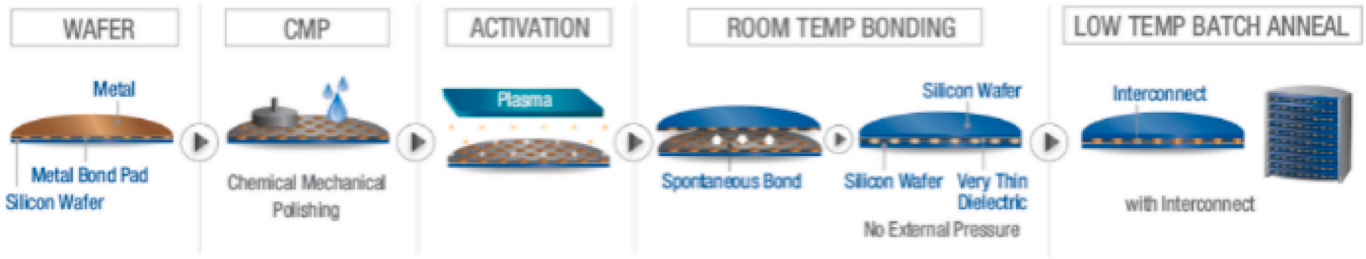


Fig. 8. The process of hybrid bonding: CMP, activation, pre-bonding and annealing [14].

and advancement of this technique. The ongoing enhancement and adjustment of this equipment are crucial for the progress of integrated circuit packaging, facilitating the development of increasingly intricate, effective, and high-performing semiconductor devices.

4. The process flow of hybrid bonding

The optimization and innovation of hybrid bonding processes are crucial for achieving small pitch, high density, and low power interconnects. As the application scenarios of hybrid bonding technology expand, the demands on the process continue to increase. Consequently, researchers are exploring more advanced, flexible, and efficient hybrid bonding processes to meet these increasing application requirements.

Hybrid bonding has evolved from the ZiBond® direct bonding technology [48]. In 2016, Sony Corporation obtained the patent license for Ziptronix's DBI® bonding technology [49] and announced the development of stacked back-illuminated CMOS image sensors (BI-CIS, Fig. 7) using Cu/SiO_2 hybrid bonding technology. In the stacked CMOS image sensors, Cu connection pads were added to both the bottom circuit chip and the top pixel chip, establishing physical and electrical connections. Subsequently, manufacturers began adopting and developing hybrid bonding processes to apply in CPUs, GPUs, and high-performance computing through 3D packaging.

The hybrid bonding process encompasses four essential stages: Chemical Mechanical Polishing (CMP), surface activation, room-temperature alignment pre-bonding, and low-temperature annealing (Fig. 8). CMP is a key technology to achieve local and global wafer surface flatness. It combines the chemical corrosion of polishing fluid and the mechanical grinding between abrasive and polishing pad to achieve the flatness of the bonding surface and the control of the metal sag size. Surface activation is a process aimed at enhancing the surface state of wafers, thereby reducing the barriers to effective bonding. Plasma activation has emerged as the predominant method for this purpose. It employs plasma generated from gases such as O_2, N_2, H_2, or Ar, which increase the hydrophilicity of the wafer surface, a critical factor for successful bonding. The subsequent stage involves alignment and pre-bonding of the activated wafers at room temperature. This step is crucial for achieving ultra-fine pitch hybrid bonding, with the bonding pitch depending heavily on the precision of wafer alignment and the capabilities of the bonding equipment employed. The final phase is high-temperature annealing, which facilitates the diffusion bonding of copper.

The chemical aspect of the CMP is primarily influenced by the polishing slurry, which usually consists of abrasive particles and chemical activators. These components interact with the wafer surface, resulting in the formation of a softer layer that can be easily mechanically removed. In the mechanical aspect, force is applied between the polishing pad and the moving slurry. Abrasive particles trapped between the wafer and the pad work to mechanically eliminate the chemically weakened surface layer. The combination of chemical and mechanical processes is crucial for effective removing material while preserving the desired surface properties and structural integrity.

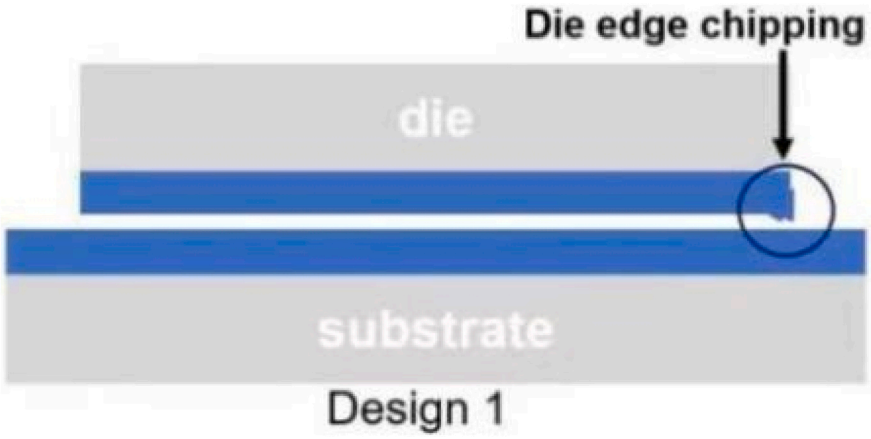


Fig. 9. Edge recess process in blade dicing diagram [56].

Jianfeng Luo and David A. Dornfeld [50] conducted thorough investigations into the CMP polishing mechanism via experimental and simulation methods. They established a wear mechanism under solid-solid contact conditions and developed a model that incorporates various process parameters such as pressure, velocity, and other critical inputs like wafer hardness, pad hardness, pad roughness, abrasive size, and geometry. This comprehensive model serves as a tool to predict material removal rates, offering a theoretical foundation for refining the CMP process.

In the context of hybrid bonding, CMP necessitates precise control over several factors to achieve optimal outcomes. Research conducted by Bahar team [51] brought forth new insights and methodologies for CMP in hybrid bonding. They identified key parameters such as slurry composition, pH value, polishing duration, and applied pressure were identified as vital to the process's efficiency and outcome. Through meticulous optimization of these elements, improvements in polishing speed, surface planarity, bonding strength and a deeper understanding of material removal selectivity were realized.

In terms of polishing fluids, Fei Qin [52] developed an innovative approach to address issues like pH instability and particle aggregation. The introduction of inorganic acids, such as sulfuric and nitric acids, as additives serves dual purposes: they regulate the pH, maintaining an ideal chemical environment, and act as novel dispersants, ensuring even distribution of abrasive particles. This unique formulation augments the stability of polishing fluid, thus avoiding uneven polishing results that could arise from fluctuations in fluid properties.

Further explorations in CMP optimization for hybrid bonding across various applications have led to enhanced performance and reliability. Basim G. Bahar's investigation into packaging-level CMP [53] focused on material selection and removal characteristics, assessing CMP slurry effects through electrochemical and surface energy evaluations. Woonki Shin et al. [54] developed a CMP process for MEMS, involving the deposition of a protective oxide layer and subsequent partial removal using a low-selectivity slurry. This approach facilitated local and global surface flattening, making it applicable in multi-level MEMS device fabrication. Xperi Corporation [55] tackled the challenge of increasing recess size in Cu CMP processes within DBI® direct bonding interconnect technology, devising a specialized CMP process that produces shallow and uniform Cu recesses on 200 mm wafers. This optimized approach enables high-quality hybrid bonding, mitigating the risk of void formation.

Post-CMP, wafer surfaces achieve an extremely low roughness, reaching angstrom levels, which is crucial for ensuring surface planarity and optimal contact for bonding. In W2W hybrid bonding, two CMP-treated wafers can undergo bonding following activation. However, in D2W bonding, wafers need to be diced into appropriately sized chips, and the dicing process may introduce defects such as chipping and particle contamination. Therefore, selecting an appropriate dicing method becomes critical in influencing subsequent die-to-wafer bonding. Common dicing techniques include blade dicing, stealth laser dicing, and plasma dicing. Research conducted by UCLA's Ren [56] introduced an edge recess technique in blade dicing, as shown in Fig. 9. The technique helps mitigate edge-related defects like chips and cracks that often arise during chip cutting process, thereby enhancing the overall bonding strength and integrity.

To address the drawbacks associated with blade dicing, DISCO has developed two methodologies: Dicing before Grinding (DBG) and Stealth Dicing before Grinding (SDBG). The DBG process involves initial semi-cutting of the wafer, followed by back-grinding to fully separate the individual chips. SDBG, an advancement of DBG, incorporates Stealth Dicing (SD) technology during the cutting stage. This technique utilizes a laser to induce internal cracks within the wafer, subsequently complemented by back-grinding. This approach is particularly effective in circumventing the defects typically associated with mechanical stress and the cutting process. Moreover, plasma dicing represents a dry etching technique that employs fluorine plasma to etch materials within the dicing lanes separating the chips. Compared to traditional blade or laser cutting, plasma dicing significantly reduces particle generation during the cutting phase, enhances yield, provides greater design flexibility, and is widely recognized as a preferred solution within the semiconductor industry. Overlooking OM images and sidewall tilt SEM images are shown in Fig. 10.

Fumihiro Inoue et al. conducted evaluations of various dicing technologies and their impacts on D2W bonding [57]. These techniques included blade dicing, laser grooving combined with plasma dicing (LG + PD), laser grooving coupled with stealth dicing (LG + SD), and laser grooving from the backside (LG from backside). It was observed that blade dicing was ineffective in achieving overall satisfactory direct bonding in D2W configurations due to the presence of particles after cutting. In contrast, LG + PD and LG from backside methods achieved successful D2W direct bonding. In the case of LG + SD, bonding at the chip edges was compromised due to laser recasting during the grooving process. Fig. 10 illustrates these differences: blade dicing resulted in debris of several tens of microns and larger backside notches, while LG + PD and LG + SD formed a step near the surface due to laser grooving. The sidewalls in LG + PD exhibited a wavy morphology owing to repeated etching and passivation in dual deep etching processes, and laser damage was evident on the sidewalls in LG + SD. Furthermore, when laser grooving was performed from the backside, the cutting was completed before transferring to the dicing lane, leading to visible mold misalignment due to mold movement during installation.

To enhance the reactivity of hybrid bonding, the activation of wafers and chips is necessary. The Suga research group from the University of Tokyo pioneered the Surface Activation Bonding (SAB) technology. Its

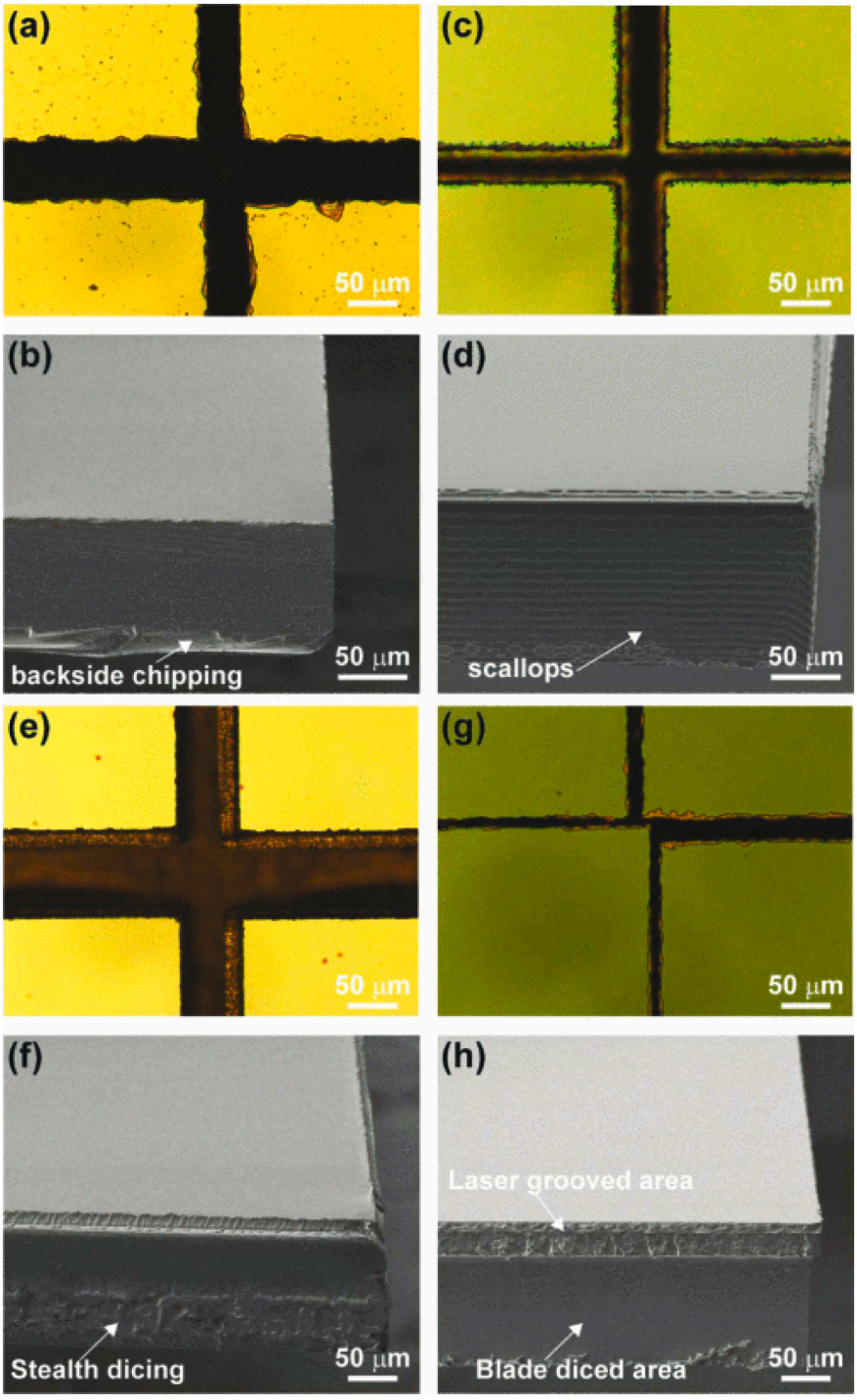


Fig. 10. Overlooking OM images and sidewall tilt SEM images (a) and (b) blade cutting, (c) and (d) LG + PD, (e) and (f) LG + SD, (g) and (h) LG from backside [57].

core mechanism involves using high-speed Ar atomic or ion beams to remove organic substances from the wafer surface, significantly enhancing its surface activity. In a high vacuum environment, this technology facilitates atomic-level contact, thus achieving highly stable interface bonding, as depicted in Fig. 11 [58–60]. While this method can achieve bonding at room temperature, its requirement for high vacuum conditions ($<5 \times 10^{-6}$ Pa) heavily depends on the equipment, posing challenges for large-scale production.

Advancing from the Surface Activation Bonding (SAB) technology, a novel approach involving low-vacuum plasma activation has emerged as the predominant and extensively adopted method for surface activation. This technique typically employs plasma sources, such as oxygen, argon, and nitrogen, to bombard the wafer surface. The plasmas effectively disrupt Si—O bonds in silicon dioxide, creating Si-OH dangling bonds. Upon contact between the opposing wafers, these Si-OH groups swiftly engage in a condensation reaction, forming Si-O-Si bonds, which facilitate the bonding of the dielectric layers. However, it should be noted that plasma activation may marginally influence surface roughness and microstructure. Which are critical for achieving the required surface precision in hybrid bonding. Additionally, this method presents challenges in addressing issues with oxidized copper, indicating that relying solely on plasma activation may not comprehensively satisfy the

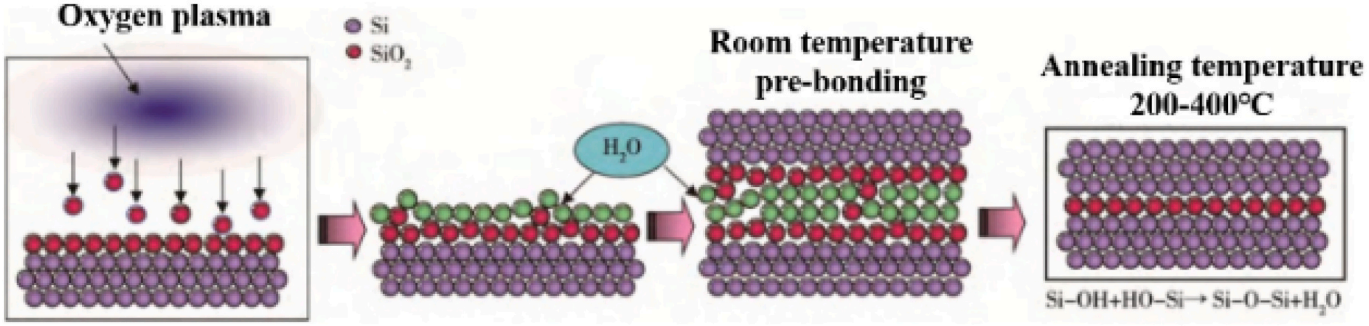


Fig. 11. Principle of plasma activation bonding [58].

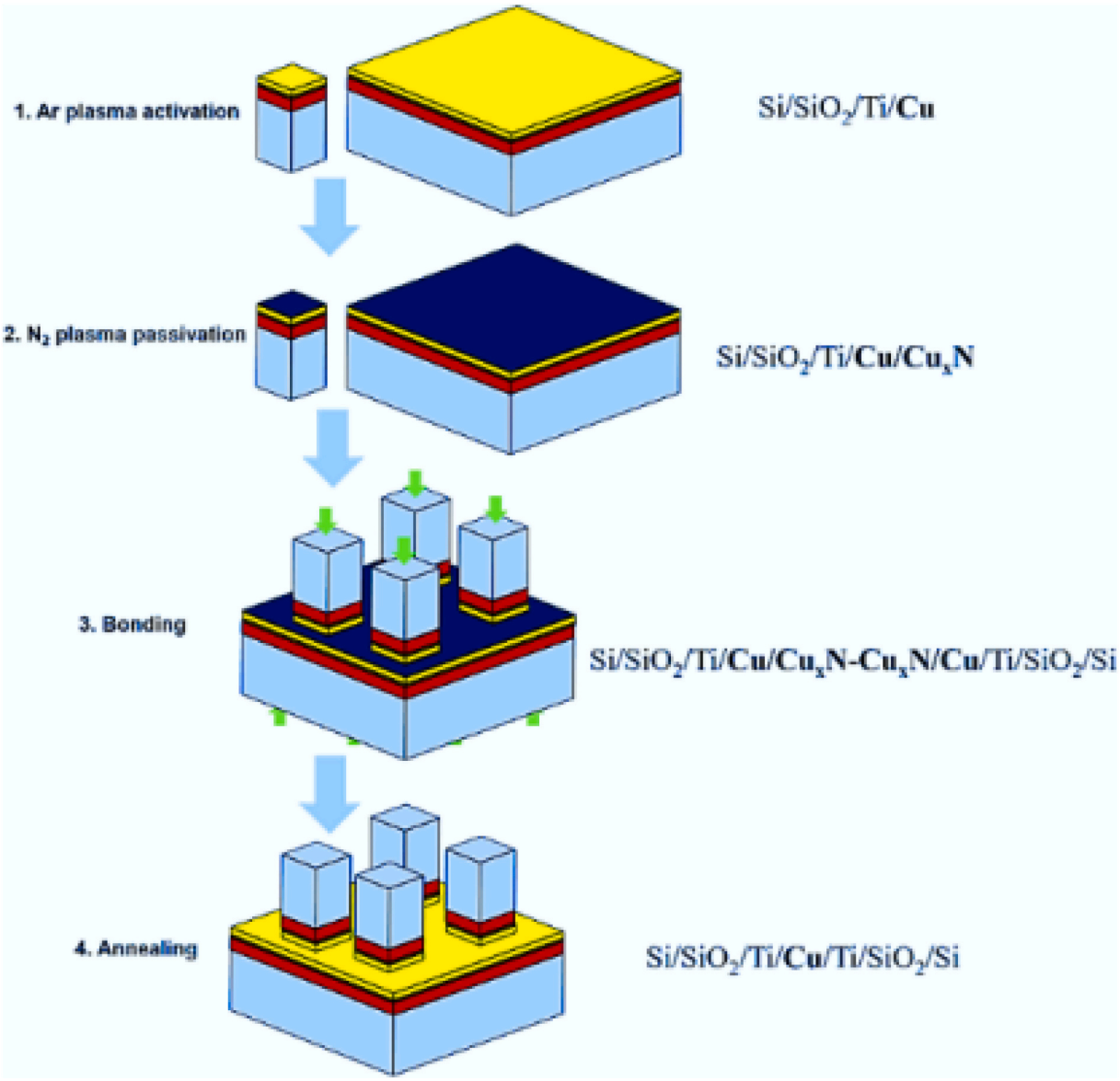


Fig. 12. The bonding processes of multi-die to wafer bonding through Ar/N_2 plasma-activated Cu—Cu direct bonding [64].

requirements for wafer surface quality in low-temperature hybrid bonding scenarios.

Chenxi Wang et al. from Harbin Institute of Technology conducted a study on the bonding method for silicon and quartz glass wafers using continuous wet chemical surface activation, specifically SPM → RCAl cleaning. Through multi-step annealing at 200 °C, they successfully achieved a strong bond without any voids or micro-cracks [61]. Additionally, they proposed the utilization of oxygen inductively coupled plasma (ICP) to eliminate organic matter and activate the surface, resulting in a reliable and tight direct bonding process [62].

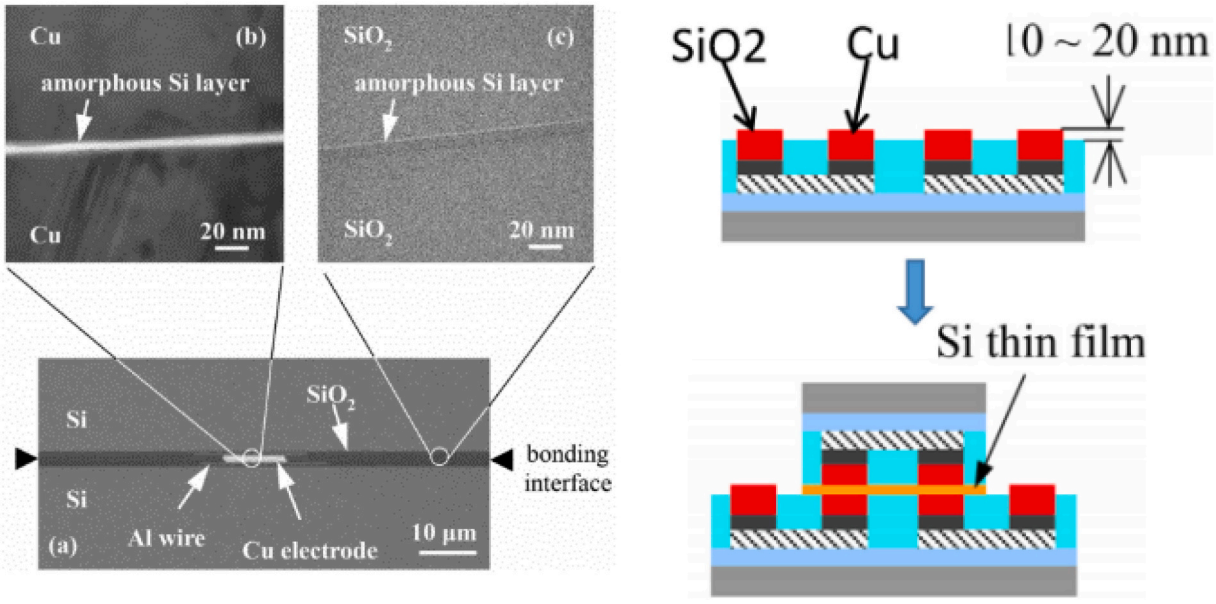


Fig. 13. Morphology of Cu-SiO_2 mixed bonding interface at room temperature [67].

Furthermore, by pre-decomposing organic components, pressure-free sintering of silver nanosize was accomplished.

Junsha Wang's research group at Meisei University Tokyo has enhanced the surface activated bonding (SAB) technique by proposing a pre-bonding baking process at 110 °C [63], which effectively eliminates adsorbed water from the silicon wafer surface and facilitates the formation of atomic bonds at the bonding interface. As a result, this advancement significantly enhances the bonding strength of SAB.

Chuan Seng Tan's team at Nanyang Technological University in Singapore explored a technique for activating the Cu surface using Ar/N_2 plasma. This approach notably diminished the hydrophilicity and roughness of the Cu surface [65]. The introduction of N_2 promoted the formation of a CuxN layer on the Cu surface, effectively preventing copper oxidation. After an annealing process at 300 °C for an hour, the bonded chips and wafers demonstrated a shear strength of 0.23 MPa, as depicted in Fig. 12. Sarah Eunkyung Kim's group at Seoul Science and Technology University in South Korea further applied this methodology to Cu-SiO_2 hybrid bonding. They observed that the Ar/N_2 plasma

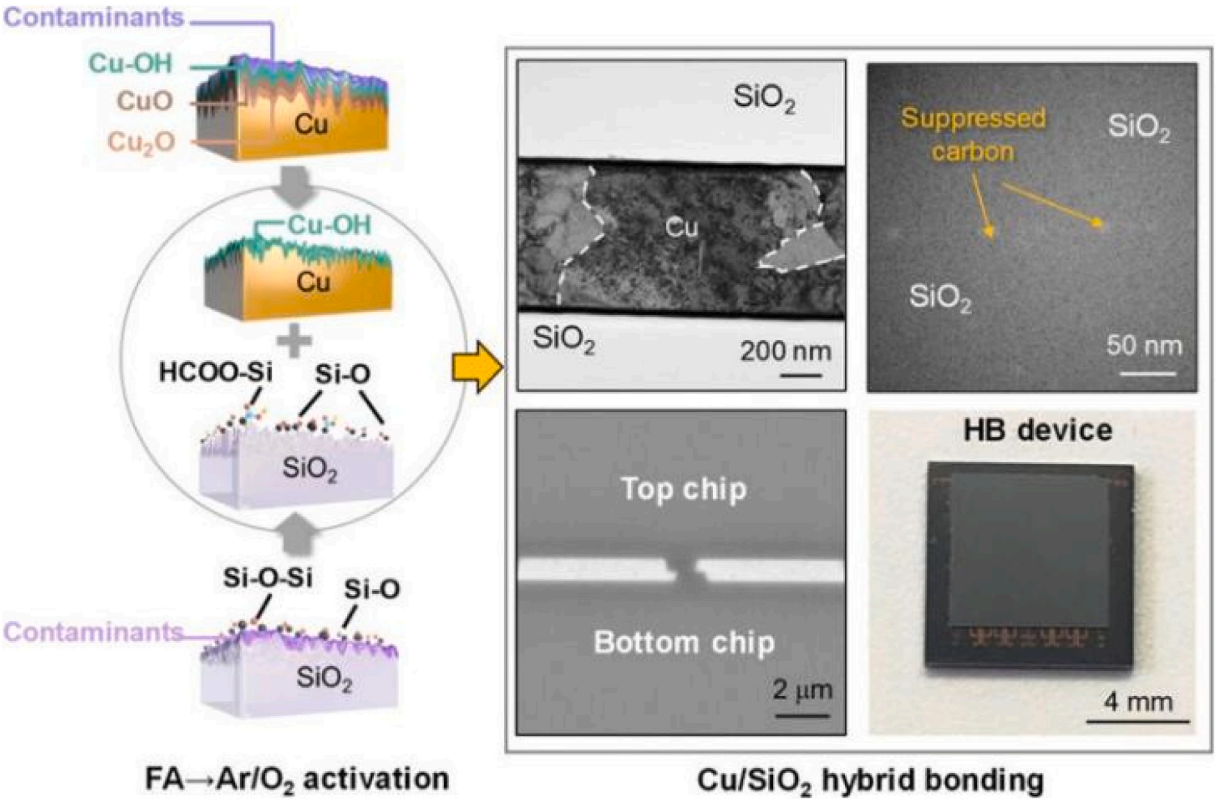


Fig. 14. Two-step activated Cu-SiO_2 hybrid bonding process and bonding interface morphology [68].

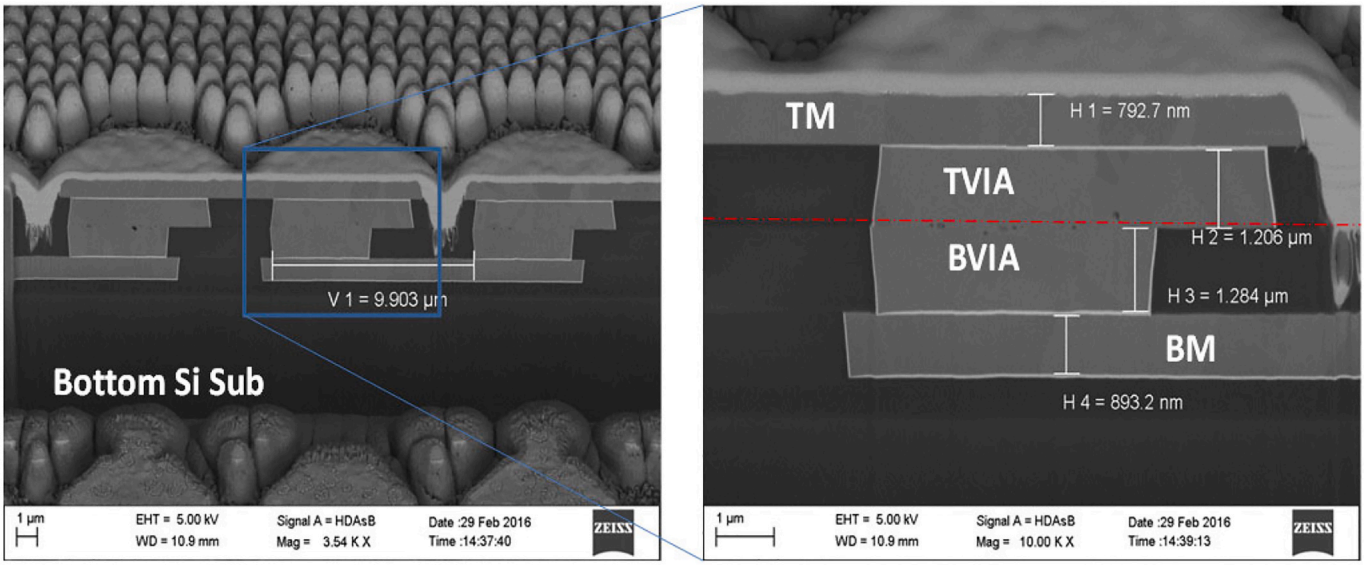


Fig. 15. SEM morphology of Cu-SiO_2 hybrid bonding interface [72].

activation led to the emergence of Si—N dangling bonds on the SiO_2 surface, enhancing the suitability for dielectric layer bonding [66]. This method offers a viable means of mitigating oxidation in metallic copper.

Jun Utsumi from Mitsubishi Corporation in Japan, successfully utilized Si ultra-thin film surface activation technology to achieve gap-free hybrid bonding of Cu-SiO_2 at room temperature [67]. The bonding interface revealed a Si thin film layer of approximately 5 nm thickness (as shown in Fig. 13), achieving a seamless connection within the dielectric layer at room temperature. The contact resistance, measured at 4.1 Ω, is relatively high for a metal layer. Using Si ultra-thin film bonding surface activation technology improved the affinity between interfaces, thereby enhancing the overall bonding quality. Despite the low Cu—Cu contact resistance, the overall contact resistance of the metal layer remains high within the entire circuit, potentially impacting the performance of electronic devices.

Addressing the issue of copper oxidation layers caused by plasma activation, the team led by Wang Chenxi at Harbin Institute of Technology [68,69] proposed a two-step cooperative activation scheme for Cu-SiO_2 based on plasma activation. This method involved the initial utilization of Ar/N_2 plasma for activation, followed by the removal of the copper oxide layer using formic acid or ammonia solution. Through the two-step activation, the surfaces of Cu and SiO_2 both exhibit a uniform distribution of -OH groups. Low-temperature hybrid bonding was achieved at 200 °C under a pressure of 2.5 MPa (as shown in Fig. 14), with the bonded area reaching approximately 80 % according to the results from Scanning Acoustic Tomography (SAT). This two-step activation scheme partially addresses the issue of copper oxidation.

Zhang Shuye et al. from Harbin Institute of Technology investigated the successful bonding of Cu—Cu pad using citrate-coated nano-silver paste in ambient air [70]. The study determined that the optimal bonding conditions for the brazing pad involve washing it three times, holding it under 1 MPa pressure and at a temperature of 260 °C for 30 min. The bond exhibits excellent thermal stability at 150 °C but experiences a significant decrease in strength at 250 °C due to substantial oxidation occurring at the interface between the Ag nanoparticle paste and the Cu pad.

The bonding of copper sintered in PT-catalyzed formic acid vapor at low temperature was investigated by Mu Fengwen from the University of Tokyo [71]. Following cleaning with acetone, ethanol, and citric acid, treatment with Pt-catalyzed formic acid vapor significantly enhances the bond strength of Cu, resulting in a denser interfacial microstructure and approximately 7 % porosity. Moreover, it imparts greater oxidation tolerance to the surface. This approach effectively overcomes the issue of easy oxidation encountered during nano-Cu slurry sintering.

The Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS) successful achieved wafer-level bonding with a pitch of 10 µm by conducting Cu-SiO_2 hybrid bonding on 12-in. (300 mm) wafers (as depicted in Fig. 15) [72]. After thinning one of the bonded wafers, electrical characterization was conducted using interconnected daisy chains and Kelvin structures. The average resistance of a single chain node was approximately 58.5 milliohms. For 5 µm contact nodes, the Kelvin contact resistance was measured about 3.49 milliohms, and the bonding contact resistance was around 68.5 milliohms, which is lower than that reported in previous studies. No significant voids or defects were observed at the bonding interface, indicating effective bonding with a bonding strength of 2.0 J/m^2.

The pre-bonding process following surface activation is of utmost importance in hybrid bonding, since it plays a vital role in creating strong and durable bindings of high quality. During this stage, precise alignment of the upper and bottom wafers or dies is achieved by marker patterns to ensure accurate positioning. Once activated, the hydrophilic surfaces of the wafer or die display strong intermolecular pressures. This process enables the removal of water and the formation of the dielectric layers at room temperature, driven by the high surface energy. Ultimately, it enables the joining of the upper and bottom samples before bonding. There are two common bonding approaches in D2W hybrid bonding: collective bonding and direct bonding. Collective bonding involves initial arranging multiple dies on a temporary carrier, creating a structure similar to a wafer. This assembly is then aligned and fused along with the target wafer. The benefit of this technique comes in its ability to simultaneously perform multiple tasks, hence improving processing efficiency. Nevertheless, it requires precise positioning of all dies on the carrier at the same time, necessitating the use of sophisticated alignment technology. In contrast, direct bonding involves directly placing and aligning individual dies onto the target wafer, allowing for accurate alignment of each die. The approach is particularly suitable for applications that require high accuracy, variable dimensions, or the integration of different components. Direct bonding is typically slower than collective bonding due to the individual handling of dies. When selecting a pre-bonding method, important factors to consider include production efficiency, needed alignment precision, and the dimensions and material properties of the wafers and dies. The choice of a pre-bonding strategy may vary depending on the specific needs of various applications and products.

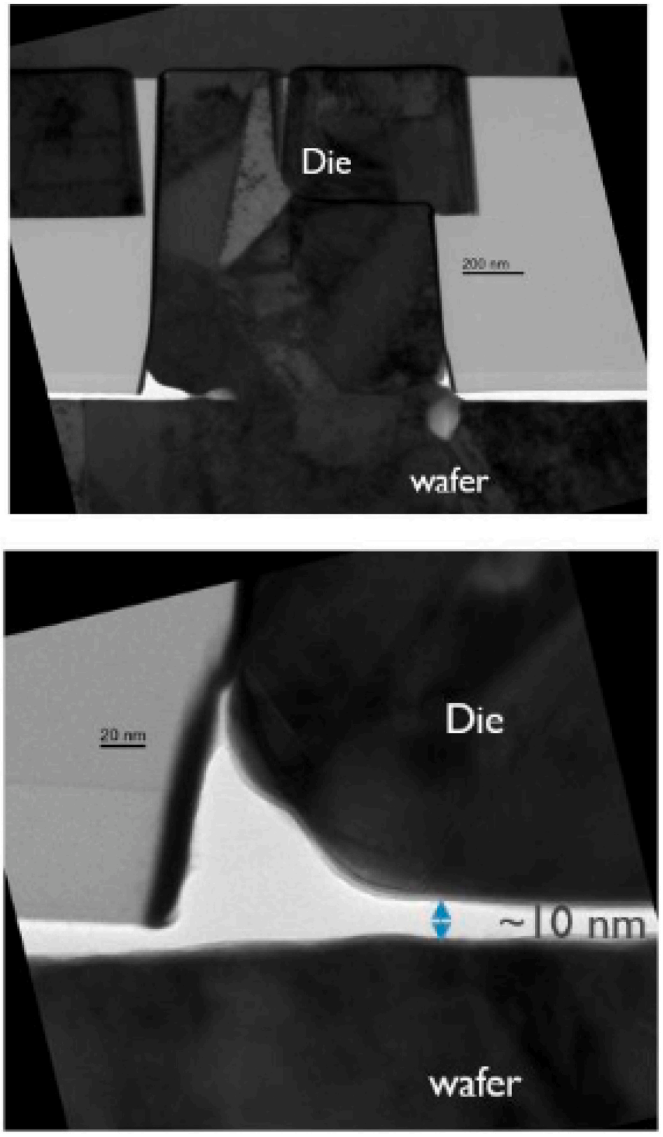


Fig. 16. TEM detection of Collective Die-to-wafer mixed bonded copper interconnect (upper layer: 40 μm spacing, lower layer: 10 μm spacing) [73].

In 2021, Interuniversity Microelectronics Centre (IMEC) proposed a collective D2W hybrid bonding method that uses a glass wafer as the carrier. The dies are pre-bonded to the carrier, followed by thinning of the glass, CMP, and pre-wafer bonding [73]. The results demonstrated a commendable bonding yield of 90 %, with 100 % yield observed in electrical structures at pitches of 40, 20, 15, and 7 μm, and 80 % yield at a 10 μm pitch. This research successfully managed the thinning of the carrier glass wafer and utilized the carrier for plasma dicing and die transfer, marking a notable advancement in hybrid bonding technology. TEM images of Collective die-to-wafer bonding results are shown in Fig. 16.

A South Korean company, Samsung, researched the use of heterogeneous dielectrics in Direct D2W hybrid bonding processes, assessing the interface characteristics of heterogeneous oxide bonding and copper-to-copper bonding [26]. Transmission Kikuchi Diffraction (TKD) was employed to confirm that grains between the upper and lower copper pads extended fully in different directions, resulting in the disappearance of interface boundary. Additionally, Electron Energy Loss Spectroscopy (EELS) analysis confirmed the absence of oxygen at the interface. The favorable characteristics of Direct D2W hybrid bonding obtained in this study contribute to further exploration of hybrid bonding processes and technological development.

AMD, an American semiconductor company, proposed a heterogeneous architecture, detailing the Direct D2W bonding technology used in their AMD 3D V-CACHE architecture [9]. This 3D V-CACHE architecture employs Direct D2W hybrid bonding processes, where known good SRAM dies are picked up and stacked sequentially on known good core chips. This approach achieves more than triple the interconnect energy efficiency, 16 times the interconnect density, improved SI/PI (Signal Integrity/ Power Integrity), lower density TSVs (Through-Silicon Vias), and decreased contact capacitance and inductance (Fig. 17).

Researchers led by Amandine Jouve [74] proposed the utilization of droplets for precise alignment in the hybrid bonding process. This method takes advantage of the minimal surface tension of the droplet, which acts as a spring-like effect until the system's energy is minimized, resulting in the minimal liquid/air surface. After the self-alignment step, direct bonding is achieved through the evaporation of the droplet. This approach successfully bonded 98 % of the dies, with 63 % of the die edges exhibiting a morphology of <5 μm. Moreover, the alignment accuracy was <1 μm (Fig. 18).

The annealing process in D2W hybrid bonding directly impacts the quality of the bond. High bond strength and void-free bond interfaces can be achieved under conventional annealing conditions at temperatures of 350 °C or higher. However, to meet the requirements of low-

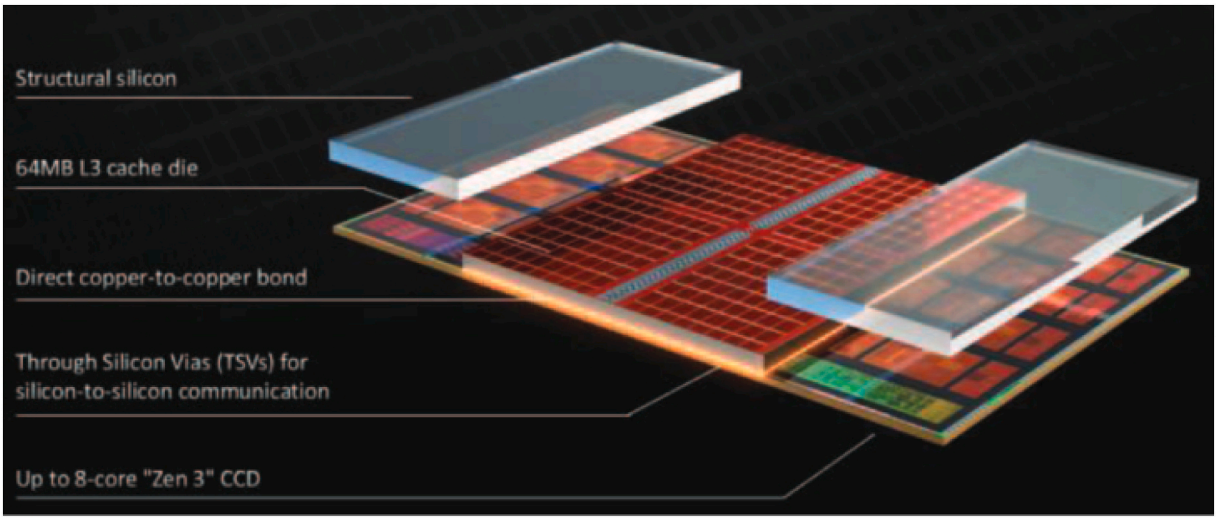


Fig. 17. Schematic diagram of AMD 3D V-Cache hybrid bonding stack chip [9].

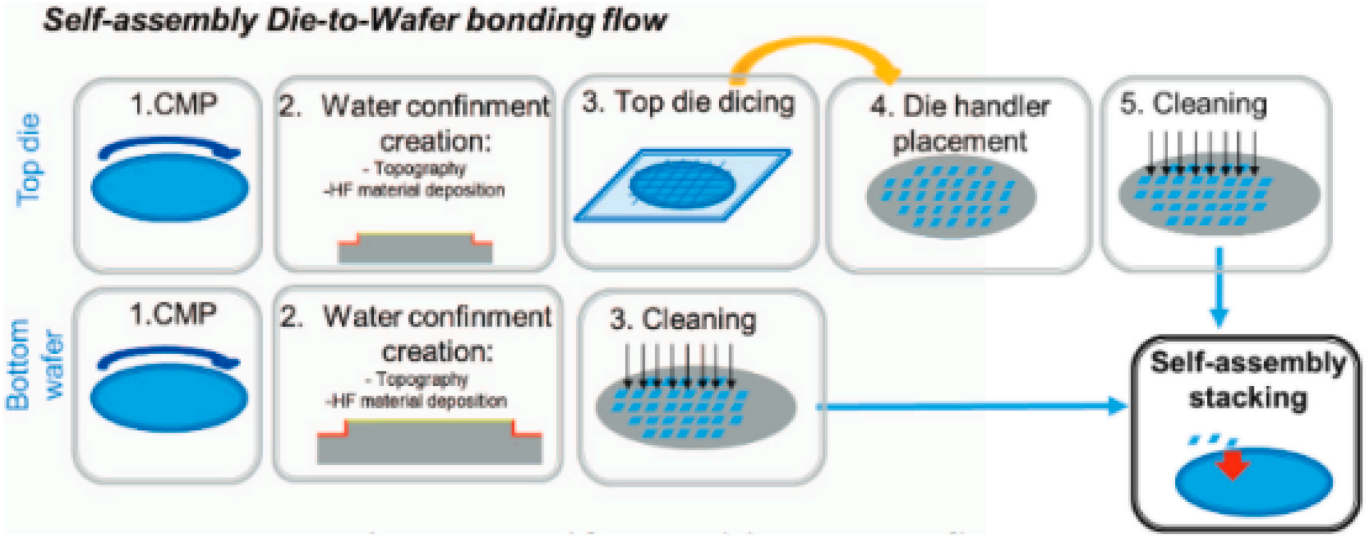


Fig. 18. Water drop self-alignment bonding process [74].

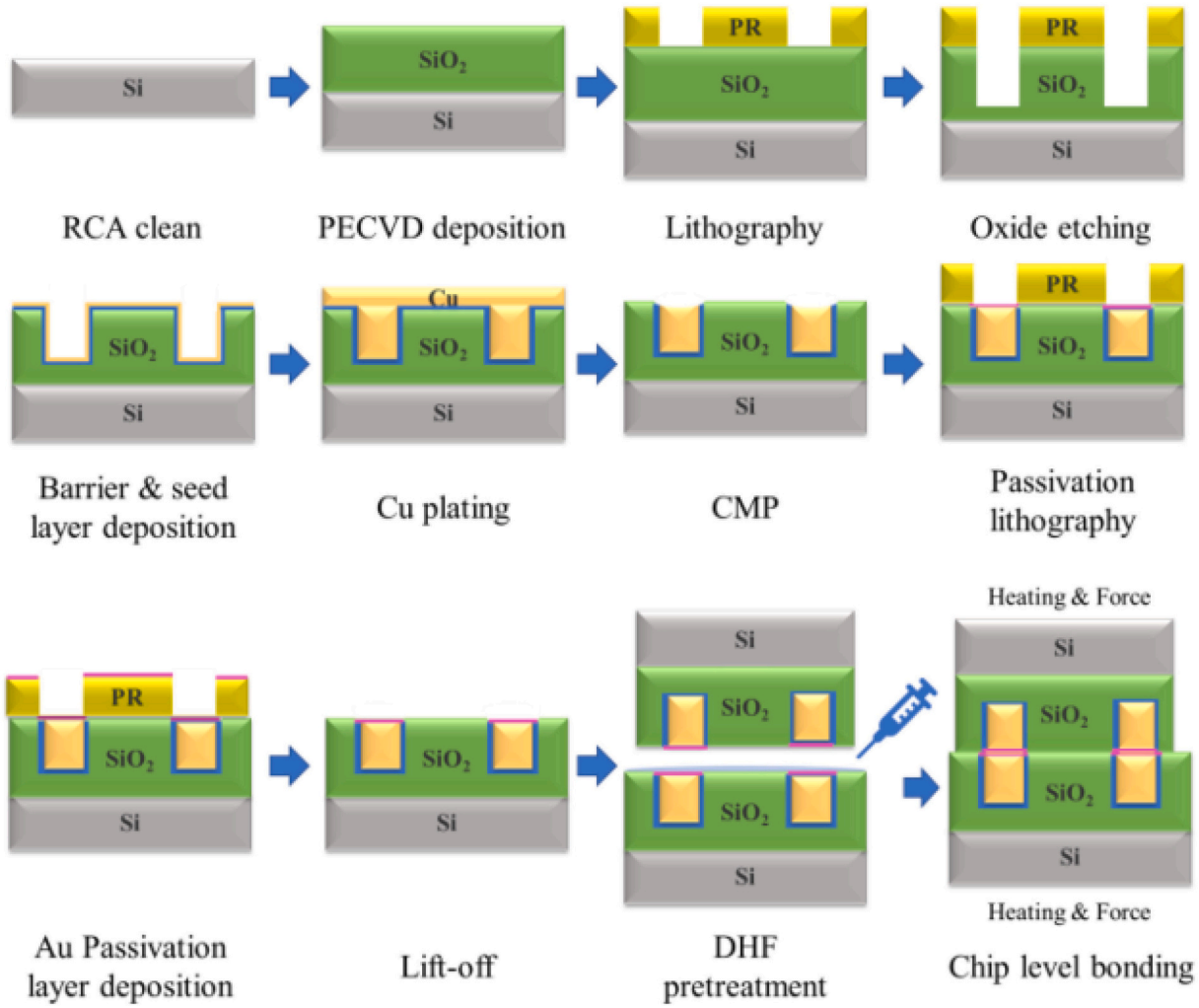


Fig. 19. Process flow of hybrid bonding with the passivation layer [37].

temperature devices, it is necessary to establish a low-temperature annealing process below 200 °C. Nonetheless, a significant issue during low-temperature annealing is the formation of numerous voids at the bond interface, which significantly reduces the yield and reliability of devices. Achieving bond strength below 250 °C that matches the fracture energy of silicon (2 J/m^2) [75] and avoiding the formation of numerous

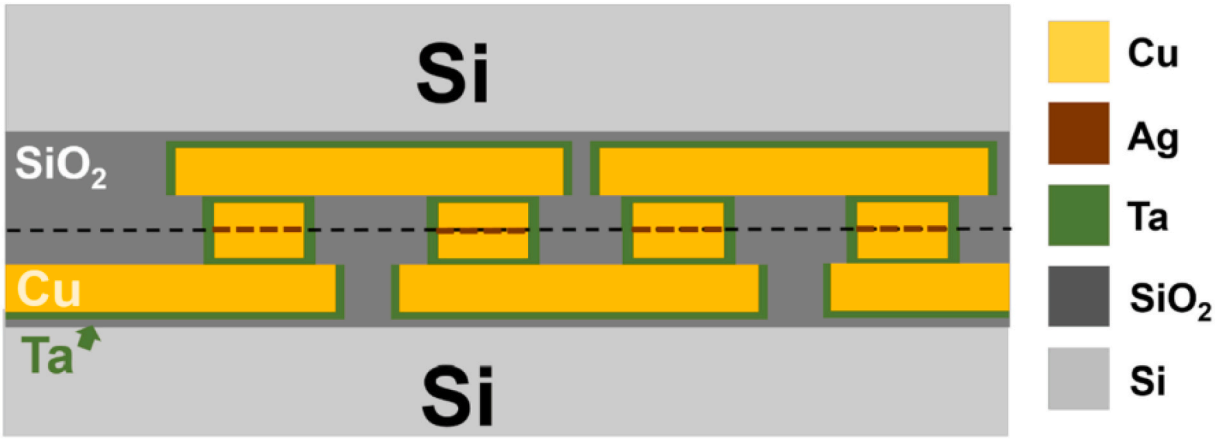


Fig. 20. Metal passivation hybrid bonding structure [40].

voids at the bond interface is an area that requires further research and optimization in the annealing process.

J. Jourdon et al. examined the impact of annealing on the electromigration characteristics of hybrid bonding [76]. They investigated various annealing conditions, including bonding anneals at different temperatures and durations, and passivation anneals in diverse atmospheres such as high-pressure deuterium (HPD_2), a hydrogen-nitrogen mix (H_2/N_2), and a control group without passivation annealing. The findings revealed that passivation annealing notably reduced electromigration lifetimes. For instance, samples annealed at 400 °C for 2 h exhibited a decrease in average failure time by 24 % and 31 % after H_2/N_2 and HPD_2 passivation annealing, respectively, indicating a significant impact of passivation annealing on electromigration lifespan.

The use of metal passivation in hybrid bonding technology can reduce the bonding temperature and improve the bonding performance. Kuan-Neng Chen et al. successfully achieved Cu/SiO_2 hybrid bonding at a low temperature of 120 °C through Au passivation and the electrical properties are optimized, resulting in excellent bonding quality, reduced thermal budget, and enhanced reliability [37]. The metal passivation structure is shown in the Fig. 19.

In 2023, Kuan-Neng Chen et al. proposed hybrid bonding of silver passivation at low temperature. The hybrid bonding of cluster-Ag passivation can reduce the bonding temperature to 120–150 °C and has excellent electrical properties [40]. This means that metal passivation has great achievements and application value in the field of reducing the hybrid bonding temperature and improve the electrical properties. The hybrid bonding structure of cluster-Ag metal passivation is shown in Fig. 20.

5. Conclusions and prospect

This paper provides a detailed introduction of key materials, bonding equipment and process steps for hybrid bonding. The selection of bonding materials, especially dielectric materials, is closely related to bonding temperature, interfacial voids and bonding energy. The exploration of new dielectric materials is expected to further reduce the bonding temperature and improve the interface bonding quality. Bonding equipment and core components serve as the fundamental basis for process development, and improving the hardware of the equipment will enhance process capabilities. In addition, the main process steps of hybrid bonding, especially CMP and activation, directly impact the bonding quality. The implementation of innovative activation methods will facilitate high-quality hybrid bonding.

To sum up, the future three-dimensional packaging will evolve towards high precision, high density and low power consumption. Through the exploration and optimization of key materials, equipment, core components, and main process nodes, the hybrid bonding technique will achieve breakthrough, thereby promoting the rapid development of three-dimensional integration.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Zhang Yu reports financial support was provided by National Natural Science Foundation of China. Zhang Yu reports financial support was provided by China Scholarship Council. Ding Fei reports financial support was provided by Beijing Superstring Academy of Memory Technology. Cao Liqiang reports financial support was provided by National Natural Science Foundation of China. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

Acknowledgements

This work is supported by the National Natural Science Foundation of China (No. 62304250, No. U21A20504), Beijing Superstring Academy of Memory Technology (No. SAMT-2022-PM02-16) and China Scholarship Council (No.202304910275).

References

[1] G.E. Moore, Cramming more components onto integrated circuits, reprinted from electronics, April 19, 1965, pp.114, IEEE Solid-State Circuits Soc. Newsl. 11 (2006) 33–35, https://doi.org/10.1109/N-SSC.2006.4785860.

[2] S. Naffziger, K. Lepak, M. Paraschou, M. Subramony, 2.2 AMD chiplet architecture for high-performance server and desktop products, in: 2020 IEEE Int. solid- state circuits Conf. - ISSCC, IEEE, San Francisco, CA, USA, 2020: pp. 44–45. doi:https://doi.org/10.1109/ISSCC19947.2020.9063103.

[3] Y. Kwon, J. Han, Y.P. Cho, J. Kim, J. Chung, J. Choi, S. Park, I. Kim, H. Kwon, J. Kim, H. Kim, W. Jeon, Y. Jeon, M. Cho, M. Choi, Chiplet heterogeneous-integration AI processor, in: 2023 Int. Conf. Electron. Inf. Commun. ICEIC, IEEE, Singapore, 2023, pp. 1–2, https://doi.org/10.1109/ICEIC57457.2023.10049867.

[4] C.C. Liu, S.-M. Chen, F.-W. Kuo, H.-N. Chen, E.-H. Yeh, C.-C. Hsieh, L.-H. Huang, M.-Y. Chiu, J. Yeh, T.-S. Lin, T.-J. Yeh, S.-Y. Hou, J.-P. Hung, J.-C. Lin, C.-P. Jou, C.-T. Wang, S.-P. Jeng, D.C.H. Yu, High- performance Integrated Fan-out Wafer Level Ppackaging (InFO-WLP): technology and system integration, in: 2012 Int. Electron Devices Meet., IEEE, San Francisco, CA, USA, 2012, https://doi.org/10.1109/IEDM.2012.6479039 (p. 14.1.1–14.1.4).

[5] L. Cao, T.C. Lee, R. Chen, Y.-S. Chang, H. Lu, N. Chao, Y.-L. Huang, C.-C. Wang, C.-Y. Huang, H.-C. Kuo, Y. Wu, H.-H. Cheng, Advanced fanout packaging technology for hybrid substrate integration, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 1362–1370, https://doi.org/10.1109/ECTC51906.2022.00219.

[6] G. Duan, Y. Kanaoka, R. McRee, B. Nie, R. Manepalli, Die embedding challenges for EMIB advanced packaging technology, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2021, pp. 1–7, https://doi.org/10.1109/ECTC32696.2021.00012.

[7] R. Mahajan, R. Sankman, N. Patel, D.-W. Kim, K. Aygun, Z. Qian, Y. Mekonnen, I. Salama, S. Sharan, D. Iyengar, D. Mallik, Embedded Multi-die Interconnect Bridge (EMIB) – a high density, high bandwidth packaging interconnect, in: 2016 IEEE 66th Electron. Compon. Technol. Conf. ECTC, 2016, pp. 557–565, https://doi.org/10.1109/ECTC.2016.201.

[8] S.F. Al-Sarawi, D. Abbott, P.D. Franzon, A review of 3-D packaging technology, IEEE Trans. Compon. Packag. Manuf. Technol. Part B 21 (1998) 2–14, https://doi.org/10.1109/96.659500.

[9] R. Agarwal, P. Cheng, P. Shah, B. Wilkerson, R. Swaminathan, J. Wuu, C. Mandalapu, 3D packaging for heterogeneous integration, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 1103–1107, https://doi.org/10.1109/ECTC51906.2022.00178.

[10] Electrical Modeling and Design for 3D System Integration: 3D Integrated Circuits and Packaging, Signal Integrity, Power Integrity and EMC | IEEE eBooks | IEEE Xplore. https://ieeexplore.ieee.org/book/6183551.

[11] B. Science, Hybrid bonding basics – what is hybrid bonding?. https://blog.brewerscience.com/what-is-hybrid-bonding.

[12] D.C.H. Yu, C.-T. Wang, H. Hsia, Foundry perspectives on 2.5D/3D integration and roadmap, 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2021, pp. 371–374, doi:https://doi.org/10.1109/IEDM19574.2021.9720568.

[13] S.W. Liang, G.C.Y. Wu, K.C. Yee, C.T. Wang, J.J. Cui, D.C.H. Yu, High performance and energy efficient computing with advanced SoICTM scaling, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 1090–1094, https://doi.org/10.1109/ECTC51906.2022.00176.

[14] DBI Wafer-to-Wafer Hybrid Bonding - Adeia. https://adeia.com/dbi-wafer-to-wafer-hybrid-bonding/, 2022.

[15] B. Appelt, T. Wang, Y. Lai, H. Chung, Next Generation fcCSP Packaging, ICEP2011 Proc, 2011, pp. 426–439.

[16] J.Q. Lü, A. Kumar, Y. Kwon, E.T. Eisenbraun, R.P. Kraft, J.F. McDonald, R. J. Gutmann, T.S. Cale, P. Belemjian, O. Erdogan, J. Castracane, A.E. Kaloyeros, 3-D integration using wafer bonding, in: D. Edelstein, G. Dixit, Y. Yasuda, T. Ohba (Eds.), Adv. Met. Conf. 2000 AMC 2000, Materials Research Soc, Warrendale, 2001, pp. 515–521. https://www.webofscience.com/wos/alldb/full-record/WOS:000177438100074.

[17] G. Katti, A. Merc, J. Van Olmen, C. Huyghebaert, A. Jourdain, M. Stucchi, M. Rakowski, I. Debusschere, P. Soussan, W. Dehaene, K. De Meyer, Y. Travaly, E. Beyne, S. Biesemans, B. Swinnen, 3D stacked ICs using Cu TSVs and die to wafer hybrid collective bonding, in: 2009 IEEE Int. Electron Devices Meet. IEDM, IEEE, Baltimore, MD, USA, 2009, pp. 1–4, https://doi.org/10.1109/IEDM.2009.5424351.

[18] V. Chidambaram, P. Lianto, X. Wang, G. See, N. Wiswell, M. Kawano, Dielectric Materials Characterization for Hybrid Bonding, 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 426–431, https://doi.org/10.1109/ECTC32696.2021.00078.

[19] K. Kennes, A. Phommahaxay, A. Guerrero, O. Bauder, S. Suhard, P. Bex, S. Iacovo, X. Liu, T. Schmidt, G. Beyer, E. Beyne, Introduction of a new carrier system for collective die-to-wafer hybrid bonding and laser-assisted die transfer, in: 2020 IEEE 70th Electron. Compon. Technol. Conf. ECTC, IEEE, Orlando, FL, USA, 2020, pp. 296–302 (doi: 10/gqjhxp).

[20] K. Sakuma, R. Yu, M. Belyansky, M.A. Bergendahl, J.-M. Gomez, S. Skordas, J. Knickerbocker, D. McHerron, M. Li, Y.M. Cheung, S. Cheung So, S.Y. Kwok, C. Ho Fan, S.W. Lau, Surface energy characterization for die-level cu hybrid bonding, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 312–316, https://doi.org/10.1109/ECTC51906.2022.00058.

[21] K.-N. Chen, S.H. Lee, P.S. Andry, C.K. Tsang, A.W. Topol, Y.-M. Lin, J.-Q. Lu, A. M. Young, M. Ieong, W. Haensch, Structure, design and process control for Cu bonded interconnects in 3D integrated circuits, in: 2006 Int. Electron Devices Meet., IEEE, San Francisco, CA, USA, 2006, pp. 1–4, https://doi.org/10.1109/IEDM.2006. 346785.

[22] F. Liu, R.R. Yu, A.M. Young, J.P. Doyle, X. Wang, L. Shi, C.T. Ryan, J.A. Hagan, K. H. Wong, M. Lu, X. Gu, N.R. Klymko, E.D. Perfecto, K.A. Kelly, S. Purushothaman, S.J. Koester, R. Wisnieff, W. Haensch, A 300-mm wafer-level three-dimensional integration scheme using tungsten through-silicon via and hybrid Cu-adhesive bonding, in: 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 2008, pp. 1–4, https://doi.org/10.1109/IEDM.2008.4796762.

[23] R.R. Yu, F. Liu, R.J. Polastre, T.M. Shaw, D. Dimilia, E.R. Kinser, A.M. Young, S. Purushothaman, S.J. Koester, W. Haensch, Reliability of a 300-mm-compatible 3DI technology based on hybrid Cu-adhesive wafer bonding, in: 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 170–171.

[24] K.N. Chen, T.M. Shaw, C. Cabral, G. Zuo, Reliability and structural design of a wafer-level 3D integration scheme with W TSVs based on Cu-oxide hybrid wafer bonding, in: 2010 Int. Electron Devices Meet, IEEE, San Francisco, CA, USA, 2010, https://doi.org/10.1109/IEDM.2010.5703283 (p. 2.4.1-2.4.4).

[25] K.-N. Chen, Z. Xu, J.-Q. Lu, Demonstration and electrical performance investigation of wafer-level cu oxide hybrid bonding schemes, IEEE Electron Device Lett. 32 (2011) 1119–1121.

[26] M.-K. Kim, S. Park, A. Jang, H. Lee, S. Baek, C. Lee, I. Kim, J. Park, Y. Jee, U.-B. Kang, D.-W. Kim, Characterization of die-to-wafer hybrid bonding using heterogeneous dielectrics, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, 2022, pp. 335–339 (doi:10/gqjhw7).

[27] S. Lee, A study on memory stack process by hybrid copper bonding (HCB) technology, in: 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 1085–1089, https://doi.org/10.1109/ECTC51906.2022.00175.

[28] J.-J. Ong, W.-L. Chiu, O.-H. Lee, H.-H. Chang, C. Chen, Low temperature Cu/SiO2 hybrid bonding fabricated by 2-step process, in: 2022 Int. Conf. Electron. Packag. ICEP, IEEE, Sapporo, Japan, 2022, pp. 135–136, https://doi.org/10.23919/ICEP55381.2022.9795579.

[29] M. Goto, Y. Honda, M. Nanba, Y. Iguchi, E. Higurashi, T. Saraya, M. Kobayashi, H. Toshiyoshi, T. Hiramoto, 3-Layer stacking technology with pixel-wise interconnections for image sensors using hybrid bonding of silicon-on-insulator wafers mediated by thin Si layers, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 122–125, https://doi.org/10.1109/ECTC51906.2022. 00029.

[30] I. Panchenko, L. Wambera, M. Mueller, C. Rudolph, A. Hanisch, I. Bartusseck, M. J. Wolf, Grain structure analysis of Cu/SiO2 hybrid bond interconnects after reliability testing, in: 2020 IEEE 8th Electron. Syst.-Integr. Technol. Conf. ESTC, IEEE, Tønsberg, Vestfold, Norway, 2020, pp. 1–7, https://doi.org/10.1109/ESTC48849.2020.9229743.

[31] Y. Zhang, J. Wang, P. Dong, X. Zhang, W. Zhao, J. Liang, M. Herkommer, K. Leyendecker, V. Wohlfarth, All copper is not created equal – examples of grain engineering in plating, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 851–855, https://doi.org/10.1109/ECTC51906.2022.00139.

[32] K.-C. Shie, P.-S. He, Y.-H. Kuo, J.J. Ong, K.N. Tu, B.T.-H. Lin, C.-C. Chang, C. Chen, Hybrid bonding of nanotwinned copper/organic dielectrics with low thermal budget, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2021: pp. 432–437. doi:https://doi.org/10.1109/ECTC32696.2021.00079.

[33] C.-C. Hsiao, H.-C. Fu, C.-W. Chiang, O.-H. Lee, T.-Y.O. Yang, H.-H. Chang, Feasibility study of nanotwinned copper and adhesive hybrid bonding for heterogeneous integration, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2021, pp. 445–450, https://doi.org/10.1109/ECTC32696.2021.00081.

[34] J.-J. Ong, D.-P. Tran, Y.-M. Hsun, W.-L. Chiu, O.-H. Lee, H.-H. Chang, C. Chen, Low thermal budget Cu/sio$_2$ hybrid bonding using highly <111>-oriented nanotwinned Cu with low contact resistivity and high bonding strength, in: 2022 17th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), Taipei, Taiwan, 2022, pp. 1–4, https://doi.org/10.1109/IMPACT56280.2022.9966728.

[35] Y.-P. Huang, Y.-S. Chien, R.-N. Tzeng, M.-S. Shy, T.-H. Lin, K.-H. Chen, C.-T. Chiu, J.-C. Chiou, C.-T. Chuang, W. Hwang, H.-M. Tong, K.-N. Chen, Novel Cu-to-Cu bonding with Ti passivation at 180°C in 3-D integration, IEEE Electron Device Lett. 34 (12) (Dec. 2013) 1551–1553, https://doi.org/10.1109/LED.2013.2285702 (doi:10.1109/LED.2013.2285702).

[36] Y.-P. Huang, Y.-S. Chien, R.-N. Tzeng, K.-N. Chen, Demonstration and electrical performance of Cu–Cu bonding at 150°C with Pd passivation, IEEE Trans. Electron Devices 62 (2015), https://doi.org/10.1109/TED.2015.2446507.

[37] D. Liu, P.-C. Chen, T.-C. Chou, H.-W. Hu, K.-N. Chen, Demonstration of low-temperature fine-pitch Cu/SiO$_2$ hybrid bonding by Au passivation, IEEE J. Electron Devices Soc. 9 (2021) 868–875, https://doi.org/10.1109/JEDS.2021.3114648.

[38] Y. Kim, S.E. Kim, Effect of the annealing process on Cu bonding quality using ag nanolayer, IEEE Trans. Compon. Packag. Manuf. Technol. 13 (2023) 737–742, https://doi.org/10.1109/TCPMT.2023.3278254.

[39] D. Liu, P.-C. Chen, Y.-W. Liu, H.-W. Hu, K.-N. Chen, Low-temperature (70°C) Cu-to-Cu direct bonding by capping metal layers, IEEE Electron Device Lett. 42 (2021) 1524–1527, https://doi.org/10.1109/LED.2021.3105434.

[40] Z.-J. Hong, D. Liu, H.-W. Hu, C.-K. Hsiung, C.-I. Cho, C.-H. Chen, J.-H. Liu, M.-W. Weng, M.-P. Hsu, Y.-C. Hung, K.-N. Chen, Low-temperature hybrid bonding with high electromigration resistance scheme for application on heterogeneous integration, Appl. Surf. Sci. 610 (2023) 155470, https://doi.org/10.1016/j.apsusc.2022.155470.

[41] Z.-J. Hong, D. Liu, S.-T. Hsieh, H.-W. Hu, M.-W. Weng, C.-I. Cho, J.-H. Liu, K.-N. Chen, Cu-Cu Room Temperature, Direct bonding using wetting/passivation scheme for 3D integration and packaging, in: 2022 IEEE Symp. VLSI Technol. Circuits VLSI Technol. Circuits, IEEE, Honolulu, HI, USA, 2022, pp. 387–388, https://doi.org/10.1109/VLSITechnologyandCir46769.2022.9830175.

[42] F. Inoue, L. Peng, A. Phommahaxay, S.-W. Kim, J. De Vos, E. Sleeckx, A. Miller, G. Beyer, E. Beyne, Characterization of inorganic dielectric layers for low thermal budget wafer-to-wafer bonding, in: 2017 5th Int. Workshop Low Temp. Bond. 3D Integr. LTB-3D, IEEE, Tokyo, Japan, 2017, p. 24, https://doi.org/10.23919/LTB-3D.2017.7947420.

[43] J. Xu, C. Wang, Q. Kang, S. Zhou, Y. Tian, Direct heterogeneous bonding of SiC to Si, SiO$_2$, and glass for high-performance power electronics and Bio-MEMS, in: 2019 IEEE 69th Electron. Compon. Technol. Conf. ECTC, 2019, pp. 1266–1271, https://doi.org/10.1109/ECTC.2019.00196.

[44] Q. Kang, C. Wang, S. Zhou, J. Xu, R. An, Y. Tian, Fabrication of Sic-on-insulator substrate via a low-temperature plasma activated bonding process, in: 2019 20th Int. Conf. Electron. Packag. Technol, 2019, pp. 1–4, https://doi.org/10.1109/ICEPT47577.2019.245118.

[45] S. Iacovo, F. Nagano, V.S.K. Channam, E. Walsby, K. Crook, K. Buchanan, A. Jourdain, K. Vanstreels, A. Phommahaxay, E. Beyne, Direct bonding using low temperature SiCN dielectrics, in: 2022 IEEE 72nd Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2022, pp. 602–607, https://doi.org/10.1109/ECTC51906.2022.00101.

[46] S. Yoneda, K. Adachi, K. Kobayashi, D. Matsukawa, M. Sasaki, T. Itabashi, T. Shirasaka, T. Shibata, A novel photosensitive polyimide adhesive material for hybrid bonding processing, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2021, pp. 680–686, https://doi.org/10.1109/ECTC32696.2021.00118.

[47] T. Suga, Status of bonding technology for hybrid integration - a review of the Surface Activated Bonding (SAB), in: IEEE Photonics Conf. 2012, IEEE, Burlingame, CA, USA, 2012, pp. 749–750, https://doi.org/10.1109/IPCon.2012.6358839.

[48] P. Enquist, 3D integration applications for low temperature direct bond technology, in: 2014 4th IEEE Int. Workshop Low Temp. Bond. 3D Integr. LTB-3D, IEEE, Tokyo, Japan, 2014, p. 8, https://doi.org/10.1109/LTB-3D.2014.6886147.

[49] Y. Kagawa, N. Fujii, K. Aoyagi, Y. Kobayashi, S. Nishi, N. Todaka, S. Takeshita, J. Taura, H. Takahashi, Y. Nishimura, An advanced CuCu hybrid bonding for novel stacked CMOS image sensor, in: 2018 IEEE 2nd Electron Devices Technol. Manuf. Conf. EDTM, IEEE, 2018: pp. 65–67.

[50] Jianfeng Luo, D.A. Dornfeld, Material removal mechanism in chemical mechanical polishing: theory and modeling, IEEE Trans. Semicond. Manuf. 14 (2001) 112–133, https://doi.org/10.1109/66.920723.

[51] G.B. Basim, Z. Ozdemir, O. Mutlu, B. Basim, Biomaterials applications of chemical mechanical polishing, in: ICPT 2012 - International Conference on Planarization/CMP Technology, Grenoble, France, 2012, pp. 1–5.

[52] F. Qin, W. Liu, Research on the manufacturing of high purity colloidal silica abrasive with controlled particle size, in: 2015 International Conference on Planarization/CMP Technology (ICPT), Chandler, AZ, USA, 2015, pp. 1–4.

[53] G.B. Basim, D. Sur, J. Langhout, Barrier and Packaging Level CMP Optimization, ECS Meet. Abstr. MA2021-01, 2021, p. 808, https://doi.org/10.1149/MA2021-0120808mtgabs.

[54] W. Shin, S. Park, H. Kim, K. Parkl, S. Joo, H. Jeong, Reduction of Dishing in Polysilicon CMP for MEMS Application by Using Protective Layer and High Selectivity, International Conference on Planarization / CMP Technology, Dresden, Germany, 2007, pp. 1–5.

[55] G. Gao, L. Mirkarimi, T. Workman, G. Guevara, J. Theil, C. Uzoh, G. Fountain, B. Lee, P. Mrozek, M. Huynh, R. Katkar, Development of low temperature direct bond interconnect technology for die-to-wafer and die-to-die applications-stacking, yield improvement, reliability assessment, in: 2018 Int. Wafer Level Packag. Conf. IWLPC, IEEE, San Jose, CA, USA, 2018: pp. 1–7. doi:10.23919/IWLPC.2018.8573278.

[56] H. Ren, Y.-T. Yang, S.S. Iyer, Recess effect study and process optimization of sub-10 μm pitch die-to-wafer hybrid bonding, in: 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 149–156, https://doi.org/10.1109/ECTC51906.2022.00034 (doi:10.11 09/ECTC51906.2022.00034).

[57] F. Inoue, A. Phommahaxay, A. Podpod, S. Suhard, H. Hoshino, B. Moeller, E. Sleeckx, K. June Rebibis, A. Miller, E. Beyne, Advanced dicing technologies for combination of wafer to wafer and collective die to wafer direct bonding, in: 2019 IEEE 69th Electron. Compon. Technol. Conf. ECTC, IEEE, Las Vegas, NV, USA, 2019, pp. 437–445, https://doi.org/10.1109/ECTC.2019.00073.

[58] R. He, M. Fujino, A. Yamauchi, T. Suga, Combined surface-activated bonding (SAB) technologies for new approach to low temperature wafer bonding, ECS Trans. 64 (2014) 83–93, https://doi.org/10.1149/06405. 0083ecst.

[59] Ran He, T. Suga, Effects of Ar Plasma and Ar Fast Atom Bombardment (FAB) treatments on Cu/polymer hybrid surface for wafer bonding, in: 2014 Int. Conf. Electron. Packag. ICEP, IEEE, Toyama, Japan, 2014, pp. 78–81, https://doi.org/10.1109/ICEP.2014.6826665.

[60] Ran He, A. Yamauchi, T. Suga, Cu/dielectric hybrid bonding using surface-activated bonding (SAB) technologies for 3D integration, in: 2014 4th IEEE Int. Workshop Low Temp. Bond. 3D Integr. LTB-3D, IEEE, Tokyo, Japan, 2014, p. 12, https://doi.org/10.1109/LTB-3D.2014.6886151.

[61] C. Wang, J. Xu, X. Zeng, Y. Tian, C. Wang, T. Suga, Low-temperature direct bonding of silicon to quartz glass wafer via sequential wet chemical surface activation, in: 2017 5th Int. Workshop Low Temp. Bond. 3D Integr. LTB-3D, 2017, https://doi.org/10.23919/LTB-3D.2017.7947417 (pp. 21–21).

[62] S. Zhou, X. Qi, Q. Kang, C. Wang, Low-temperature direct and indirect bonding using plasma activation for 3D integration, in: 2020 IEEE Int. Conf. Integr. Circuits Technol. Appl. ICTA, IEEE, Nanjing, China, 2020: pp. 130–132. doi:10.1109/ICTA50426.2020.9331985.

[63] K. Takeuchi, E. Higurashi, J. Wang, A. Yamauchi, T. Suga, Removal of adsorbed water on si wafers for surface activated bonding, in: 2022 IEEE CPMT Symp. Jpn. ICSJ, 2022, pp. 61–64, https://doi.org/10.1109/ICSJ55786.2022.10034710.

[64] L. Hu, S.C.K. Goh, Y.D. Lim, P. Zhao, M.J.Z. Lim, C.S. Tan, Multi-die to wafer bonding through plasma-activated Cu-Cu direct bonding in ambient conditions, in: 2021 IEEE Int. 3D Syst. Integr. Conf. 3DIC, 2021, pp. 1–5, https://doi.org/10.1109/3DIC52383.2021.9687609.

[65] L. Hu, S.C.K. Goh, J. Tao, Y.D. Lim, P. Zhao, M.J.Z. Lim, C.S. Tan, In-depth parametric study of Ar or N2 plasma activated Cu surfaces for Cu-Cu direct bonding, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2021, pp. 420–425, https://doi.org/10.1109/ECTC32696.2021.00077.

[66] H.K. Seo, S. Eunkyung Kim, G. Kim, H.S. Park, Y.-B. Park, Effects of two-step plasma treatment on Cu and SiO_2 surfaces for 3D bonding applications, in: 2020 IEEE 70th Electron. Compon. Technol. Conf. ECTC, IEEE, Orlando, FL, USA, 2020, pp. 1677–1683, https://doi.org/10.1109/ECTC32862.2020.00263.

[67] J. Utsumi, K. Ide, Y. Ichiyanagi, Bonding of SiO_2 and SiO_2 at Room Temperature using Si ultrathin film, ECS Trans. 75 (2016) 355–361, https://doi.org/10.1149/07509.0355ecst.

[68] Q. Kang, C. Wang, S. Zhou, G. Li, T. Lu, Y. Tian, P. He, Low-temperature co-hydroxylated Cu/SiO_2 hybrid bonding strategy for a memory-centric chip architecture, ACS Appl. Mater. Interfaces 13 (2021) 38866–38876, https://doi.org/10.1021/acsami.1c09796.

[69] Q. Kang, G. Li, F. Niu, C. Wang, Cooperative surface-activation strategy for low-temperature Cu/SiO_2 hybrid bonding, in: 2022 IEEE Int. Conf. Integr. Circuits Technol. Appl. ICTA, 2022, pp. 40–41, https://doi.org/10.1109/ICTA56932.2022.9963057.

[70] S. Zhang, X. Duan, Z. Li, J. Xu, D. Wang, S. Zhang, P. He, K.-W. Paik, Effects of the citrate-coated nanosized Ag pastes on joining reliable Cu-Cu joints for current 3D Ics, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, 2021, pp. 1957–1962, https://doi.org/10.1109/ECTC32696.2021.00309.

[71] F. Mu, H. Ren, L. Liu, Y. Wang, G. Zou, T. Suga, Nano-Cu paste sintering in Pt-catalyzed formic acid vapor for Cu bonding at a low temperature, in: 2019 Int. Conf. Electron. Packag. ICEP, 2019, pp. 365–366, https://doi.org/10.23919/ICEP.2019.8733407.

[72] C. Song, H. Li, G. Feng, L. Cao, W. Zhang, 10μM pitch Cu-cu bonding interconnection for wafer level 3D integration, in: 2016 17th Int. Conf. Electron. Packag. Technol. ICEPT, IEEE, Wuhan, China, 2016, pp. 979–982, https://doi.org/10.1109/ICEPT.2016.7583291.

[73] S. Suhard, K. Kennes, P. Bex, A. Jourdain, L. Teugels, E. Walsby, C. Bolton, J. Patel, H. Ashraf, R. Barnett, F. Fodor, A. Phommahaxay, D. La Tulipe, G. Beyer, E. Beyne, demonstration of a collective hybrid die-to-wafer integration using glass carrier, in: 2021 IEEE 71st Electron. Compon. Technol. Conf. ECTC, IEEE, San Diego, CA, USA, 2021, pp. 2064–2070, https://doi.org/10.1109/ECTC32696.2021.00325.

[74] J. Amandine, L. Sanchez, C. Castan, M. Laugier, E. Rolland, B. Montmayeul, R. Franiatte, F. Fournel, S. Cheramy, Self-assembly process for 3D die-to-wafer using direct bonding: a step forward toward process automatisation, in: 2019 IEEE 69th Electron. Compon. Technol. Conf. ECTC, 2019, pp. 225–234, https://doi.org/10.1109/ECTC.2019.00041.

[75] R. Pelzer, V. Dragoi, P. Kettner, D. Lee, Advanced low temperature bonding technologies, in: 2004 IEEE Int. Conf. Semicond. Electron., IEEE, Kuala Lumpur, Malaysia, 2004, https://doi.org/10.1109/SMELEC.2004.1620832 (5 pp).

[76] J. Jourdon, S. Moreau, D. Bouchu, S. Lhostis, N. Bresson, D. Guiheux, R. Beneyton, S. Renard, H. Fremont, Effect of passivation annealing on the electromigration properties of hybrid bonding stack, in: 2017 IEEE Int. Reliab. Phys. Symp. IRPS, IEEE, Monterey, CA, USA, 2017, https://doi.org/10.1109/IRPS.2017.7936378 (p. MR-3.1-MR-3.6).