



Review

Materials, processing and reliability of low temperature bonding in 3D chip stacking



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ARTICLE INFO

Article history:

Received 23 January 2018

Received in revised form

21 March 2018

Accepted 3 April 2018

Available online 7 April 2018

Keywords:

3D IC

Low temperature bonding

Bonding method

Reliability

ABSTRACT

Due to the advantages of small form factor, high performance, low power consumption, and high density integration, three-dimensional integrated circuits (3D ICs) have been generally acknowledged as the next generation semiconductor technology. Low temperature bonding is the key technology to ensure the chip (or wafer) stacking in 3D ICs. In this paper, different low temperature bonding methods for chip (or wafer) stacking were reviewed and described systematically. Materials, processing and reliability will be extremely important, their effects on the 3D IC structure were addressed in detail, the challenging reliability issues may be considered as the major concern in the future work. The latest development of low temperature bonding in 3D ICs is also given here, which helpful may provide a reference for the further study of low temperature bonding.

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1. Introduction

With the development of large-scale-integration of circuits on Si

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chip technology, the use of Moore's law in microelectronic industry may approach the limit, the advanced three-dimensional integrated circuits (3D-IC) technology can overcome the limitations of the Moore's law in the continuous development of integrated circuits, in 3D IC the chip technology and packaging technology are merged closer and closer together [1–3]. 3D IC technology can enhance the high-density integrated chips to achieve powerful performance, small form factor, low power consumption, and low cost, the diameter of microbumps is now about 10–20 μm , there is enough room in 3D IC structure. Three-dimensional ICs are based on vertical integration, where two or more electronic components are homogeneously or heterogeneously stacked and can be formed by chip-to-chip, chip-to-wafer, or wafer-to-wafer stacking [4].

Yole Development in Lyon (France), has projected recently that the 3D IC market in 2017 will reach US\$38B, which is about 3–4% of the global semiconductor market of US\$1 trillion, and 3D IC has ten times faster growth than the global semiconductor industry [5], which shows the 3D IC technology may play an important role in microelectronic industry, and the market requirement may increase significantly in the future. In order to attain 3D IC structure, several key technologies have to be perfectly mastered, such as vertical interconnection by through silicon via (TSV), wafer thinning and handling, and wafer/chip stacked bonding (including chip-to-chip (C2C), chip-to-wafer (C2W) and wafer-to-wafer (W2W) bonding schemes) [6], and stacked bonding was considered as an important technology in 3D IC.

In this paper, different low temperature bonding techniques are reviewed systematically. The 3D integration samples using these bonding technologies and platforms developed in companies or research institutes are also represented, the related materials, processing and reliability are shown and reviewed respectively.

2. TLP bonding

Compared with traditional solid-state diffusion bonding (SSD) such as Al/Al and Au/Au, transient liquid phase (TLP) bonding has the advantages of relatively low temperature and short time, and has gradually become an attractive joining technique for the attachment of metals, ceramics and composites, the process employs a low melting point interlayer between the base metals to be joined and relies on interdiffusion for isothermal solidification at the bonding temperature [7–9]. In the electronic industry, solid-liquid interdiffusion (SLID) bonding is a bonding technique based on intermetallic formation [10], the concept is also known as isothermal solidification and transient liquid phase (TLP) bonding [11], which can be considered as the same processing comparing with TLP bonding, only another name. With the miniaturization development of electronic device, the volume shrink of joints in electronic device become the essential process, as shown in Fig. 1 [11]. In 3D packaging, the joints in chip stacking has a diameter of 20–10 μm and a thickness of 10–5 μm [12], so after TLP bonding, the joints only shown thermodynamically stable intermetallic compounds with high melting points [13], ensuring the later

bonding processing in chip stacking system.

2.1. Cu–Sn bonding

Cu–Sn bonding was selected obviously as the interconnect materials in 3D IC, the schematic view of Cu–Sn TLP bonding was shown in Fig. 2 [7]. Based on optimized design of Cu/Sn thickness, the Sn can be deposited on the surface of Cu substrate, using bonding at 260 $^{\circ}\text{C}$ for 30 min the Cu–Sn/Cu structure can be joined together, during the bonding Cu substrate will react with the molten solders to form Cu_6Sn_5 firstly [14], after Sn is depleted, the formation and growth of Cu_3Sn between Cu_6Sn_5 and Cu substrate, the Cu_3Sn is governed by the phase stability according to the reaction: $\text{Cu}_6\text{Sn}_5 + 9\text{Cu} \rightarrow 5\text{Cu}_3\text{Sn}$ [15,16]. Therefore, after bonding only Cu_3Sn intermetallic compounds exist in the joints.

Cu–Sn TLP bonding can be used in high-temperature power electronics packaging [17]. In the bonding structure, 200 μm -thick Cu coupons and 7 μm thick Sn layer were selected in the TLP bonding (N_2 , 300 $^{\circ}\text{C}$). Fig. 3 shows the SEM pictures of Cu–Sn and Ni–Sn TLP bonded joints, the typically scallop-type Cu_6Sn_5 were found at both interface during reflow processing in Cu–Sn bonding, Zhang [18] also found that a monolayer of scallop-type Cu_6Sn_5 grains (2 μm in diameter) in Cu–Sn3.0Ag0.5Cu–Cu lap-type interconnects, the similar phenomenon can be found in SnPb–Cu and SnAg–Cu solder joints [19]. After Cu–Sn bonding for 30 min, the Cu_3Sn can be observed at the interfaces between Cu_6Sn_5 and Cu. With the further increase of duration, the Sn can be consumed completely, only Cu_6Sn_5 and Cu_3Sn can be observed after 2 h bonding, when the TLP bonding time is 3 h, the thickness of Cu_3Sn layer increases obviously. However, in the SEM figures, the voids can be found evidently, which can reduce the reliability of bonded joints in services, especially for service life. Lucase [20] found the Kirkendall voids can form seminal cracks that adversely affect the joint reliability. Liu [21] demonstrated that a through crack propagated across the microbump after being annealed for 1000 h at 150 $^{\circ}\text{C}$, and the voids can be observed in the crack. So the control of voids formation in Cu–Sn bonded joints should be an important aspect in 3D IC to enhance the reliability of 3D structure.

Tin (50 μm thick) was used to form joints between two Cu foils (0.25 mm thick), the couples bonded at temperatures between 275 and 325 $^{\circ}\text{C}$ (15 min–48 h) [22], during 325 $^{\circ}\text{C}$ bonding, Cu_6Sn_5 phases grow into molten tin from both Cu substrates, when the bonding time increase, the Cu_3Sn can be observed. At extremely long reaction times (5 h), only Cu_3Sn phase is present. Once the Cu_3Sn phase has extended to the whole structure of joints, no further changes in phase appear to occur after still longer reaction times. Gagliano [23] calculated the kinetic exponents and activation energies, found that thickening of the Cu_6Sn_5 was controlled by a grain-boundary diffusion mechanism, and the growth of the Cu_3Sn occurs by solid-state diffusion, probably grain-boundary diffusion. For the calculation of activation energies, different authors give various data, the discrepancy among the activation energies are due to differences in the diffusion couple methods, aging conditions and analytical method used [24]. In addition, when the bonding temperature is so higher, the phase in the bonded joints will change, for example, bonding was performed at 400 $^{\circ}\text{C}$ for 4 h, these conditions produced a uniform layer of the $\text{Cu}_{41}\text{Sn}_{11}$, without Cu_6Sn_5 , Cu_3Sn or Sn, and without porosity [25]. The intermetallic compound growth in Cu/Sn/Cu sandwich structure under transient liquid phase bonding conditions can be simulated using multiphase-field method [26], the intermetallic compound evolution can be reasonably predicted in advance of experimental studies.

Cu–Sn TLP bonding was used in MEMS wafer-level packaging, bonding temperatures ranged from 240 $^{\circ}\text{C}$ to 280 $^{\circ}\text{C}$, the pressure is

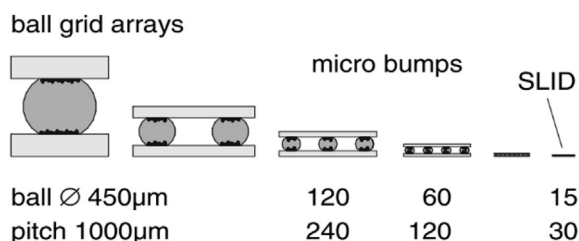


Fig. 1. vol shrinks of joints [11].

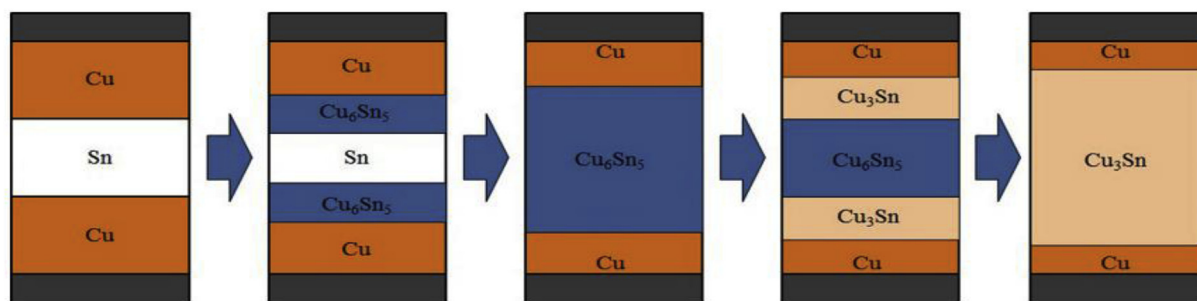


Fig. 2. Schematic view of Cu/Sn TLP bonding [7].

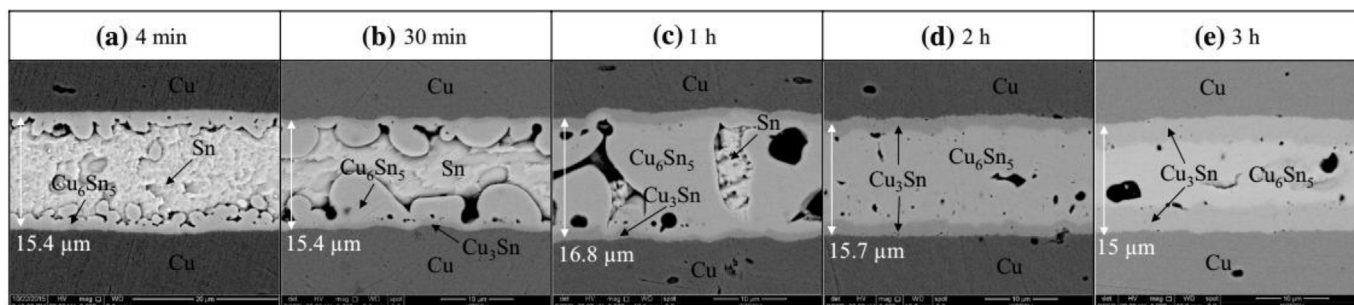


Fig. 3. Cross-sectional SEM micrographs of Cu–Sn–Cu TLP bonding with various durations [17].

130 MPa, the shear strengths after bonding were about or even higher than 100 MPa, and meet the requirement of the MIL-STD-883G in all cases [27]. Cu/Sn–Cu bonding (270 °C, 300 °C, pressure: 5×10^6 kg/m²) was conducted at 10 μm and 15 μm pitch in large area arrays, as shown in Fig. 4 [28]. During thermal cycling testing, bonded samples show no significant changes in the electrical yield or channel resistance. Lee demonstrated that electrical resistance was not very sensitive to the bonding conditions, indicating that the microstructure evolution and changes in the bonding morphology do not significantly influence the resistance [29]. Moreover, Cu–Sn TLP bonding (250 °C) for 40 μm pitch peripheral array and 100 μm pitch area array with greater than 90% electrical yield has been demonstrated, the fracture mode of bonded joints is fracture through the intermetallic compound [30]. In order to improve the Cu–Sn bonded joints (225–300 °C, pressure: 1.26 MPa), 10-nm Ni buffer layer was selected to suppress immense Cu/Sn interdiffusion rate during heating step enhances the mechanical strength significantly [31]. Robust bond strength and reliable electrical property represent obviously.

2.2. Cu–Sn (additives) bonding

In order to improve the Cu–Sn bonded joints, the alloying method was selected to develop new Sn base materials for 3D chip stacking, which has been utilized effectively in lead-free solders [32–36]. Based on the additives, the microstructures and properties of Cu–Sn bonded joints can be enhanced obviously. Cu particles (30 μm in diameter) was selected by Chen [37] as additive, which were dropped into the chemical tin plating solution and coated with a Sn layer approximately 2–3 μm in thickness, then pressed into preforms. The new interconnect materials bearing Cu particles can be reflowed at a low temperature (<260 °C) due to the low melting temperature of the outer Sn layer. Fig. 5 shows the schematic diagram of the TLP bonding process based on a preform fabricated with Cu@Sn particles, during the long time bonding, Cu particles can react with Sn to form Cu₆Sn₅ firstly, then to form Cu₃Sn between Cu₆Sn₅ and Cu, so the Cu₆Sn₅ and Cu₃Sn

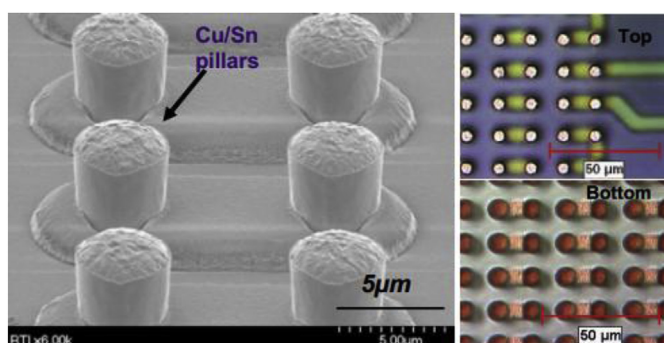


Fig. 4. (left) SEM of top die with tin plated pads and (right) optical microscope images of the top and bottom die [28].

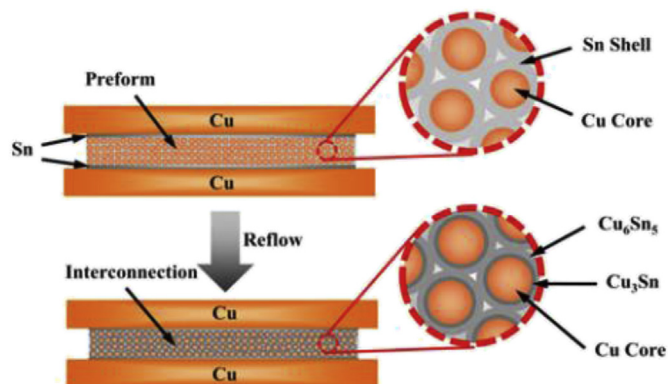


Fig. 5. Schematic diagram of the TLP bonding process based on a preform fabricated with Cu@Sn particles [37].

intermetallic compounds can be observed in the bonded joints, the Cu particles were surrounded by Cu_6Sn_5 and Cu_3Sn , the bonded joints can withstand a high temperature of up to 415 °C. Fe particles (1–2 μm in diameter) as additive in SnAgCu solder were found to react with Sn, to form FeSn_2 [38], Ni particles (~5 μm in diameter) was encapsulated by Cu–Ni–Sn intermetallic compounds [39], the modification mechanism is particles strengthen. Based on the addition of particles of Cu particles in Cu–Sn bonded joints, the shear strength, electrical and thermal performance.

Due to the reaction between Cu and Sn during bonding, the bonded joints contain Cu_6Sn_5 and Cu_3Sn intermetallic compound (IMC), the rapid growth of IMC can degrade the property of joints [40]. Yang [41] selected Ag, Zn, Bi addition to modify the growth of Cu–Sn IMC, the growth kinetics of Cu–Sn reaction products (i.e. Cu_6Sn_5 and Cu_3Sn) could be effectively suppressed by means of Ag addition particularly at lower temperature, the concentrations of minor Bi will continue rising as the interfacial reactions proceeds. At the Cu/ Cu_3Sn interface, plentiful voids can be observed in Fig. 6, the addition of alloying elements cannot effectively inhibit the formation of voids. In SnAg/Cu bonding, the structure were bonded applying a temperature of 300 °C and 10 N loads [42], small voids were found in the IMC solder joints, and the voids from the fringe can be avoided with hydrogen radical treatment. For Cu–Sn TLP bonding (250 °C, 0.2 N and 50 N pressures), 0.5% CuZnAl memory particles were selected as additives [43]. It was found that with the addition of 0.5% CuZnAl memory particles, the interface reaction can be inhibited, which can be attributed to the decrease of diffusion of elements at the interface. Moreover, comparing to 0.2 N pressure, under 50 N pressure the large amount of voids can be found because of the strong diffusion of elements, no defect can be observed in solder joints with 0.2 N pressure, the uniform microstructure can be found at the interface. With the mechanical property testing, the shear force can be enhanced by 20%–25%. In order to reduce the bonding temperature for wafer bonding, Lee [44] proposed that In–Sn(50/50) alloy can be used to bond the wafers at 160 °C to form the interface of wafer bonding. Before bonding, In–Sn 12 μm and Au–Sn 100 nm films have been subsequently deposited onto the lid wafer L1 and L2. Experimental

samples were put inside a vacuum chamber, and the soldering parameters is 160 °C, 5×10^{-5} Torr, with an axial loading of 3 kg/ cm^2 for 1.5 h. The experimental results show helium leakage rate of 6×10^{-9} Torr l/s, it is found from the experiment that an interface strength can be as high as 210 kg/ cm^2 . Reliability test after 1500 temperature cycles between –10 °C and 80 °C also shows no trace of degradation compared to the initial quality of the samples, which indicated that the In–Sn solder is an ideal low-temperature inter-layer for wafer bonding.

2.3. Au–Sn bonding

Au–Sn TLP bonding is selected as excellent processing in electronic industry, in 1997, Cain have done the Au/Sn/Au TLP bonding in terms of a numerical diffusional model [45]. Au–Sn TLP bonding was used in MEMS wafer-level packaging from 240 °C to 280 °C and different dwell times from 8 to 30 min, the pressure is 130 MPa, the sample showed high shear strengths (>80 MPa) after bonding, nearly perfect bond regions and no main failure mode in the cleavage analyses, and meet the requirement of the MIL-STD-883G in all cases [27]. Bobzin [46] developed Au–Sn–Au transient liquid bonding, primarily for potential medical applications in hybrid microsystems, in the microstructure of bonded joints (after 270 °C bonding), AuSn, AuSn_2 , AuSn_4 phases can be observed respectively. The shear tests show that all tested joints have high shear strengths in the band of 40–60 MPa, good thermo-shock behavior and high corrosion resistance can be found. Lugscheider [47] reported the Au–Sn TLP bonding conditions (270 °C, 30 min), 270 °C is higher for low temperature bonding in 3D chip stacking. Moreover, the price of Au is so higher than Cu, or Ni, the using of Au–Sn bonding will increase the cost of 3D IC device.

2.4. Au–In bonding

Thin In based solder layers were chosen by Choi [48] for the low melting temperature solder and bonded to thin Au layer to form Au–In based IMC after bonding, the schematic Schematics of stacked dice fabricated by low temperature bonding was shown in Fig. 7. In order to bond a thin In film on Au pad below 200 °C, a diffusion barrier layer is needed in between Au and In layers before bonding, since the Au diffusion into In layer is fast enough to form Au–In intermetallics even at a room temperature. After design of experiments (DOE), with optimal parameters (6 MPa, 120 °C, 12 h), the Au–In based IMC solder joints was expected to show 15.5 MPa, moreover, the failure occurred along the IMC solder joints as observed by SEM testing. During the stacking process, Au–In based IMC joints were stable and successfully stacked up the next layer in the 3 layers dice without damaging the IMC joints formed in the previous stacks at 180 °C. Also, the 3-layer stacked dices could go through the reflow processes with a peak temperature of 260 °C

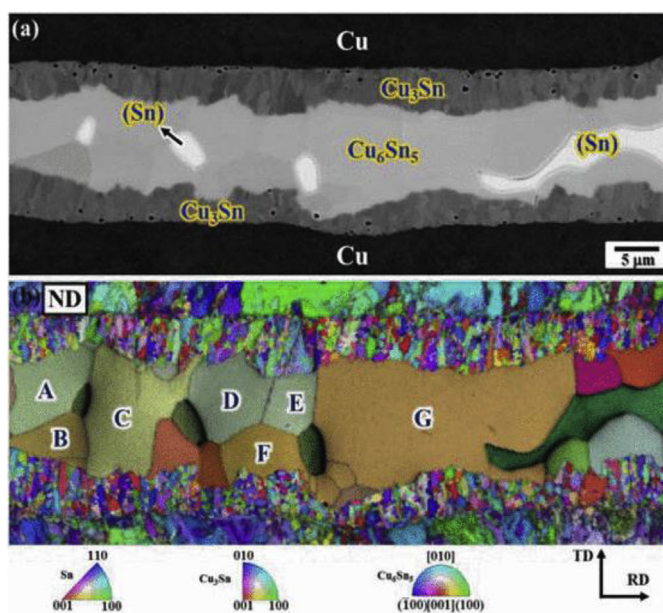


Fig. 6. (a) Cross-sectional micrograph of Cu/Sn (10 μm)/Cu sandwich aged at 180 °C for 192 h. (b) The corresponding orientation image map (image quality + inverse pole figure) of Cu_6Sn_5 , Cu_3Sn , and Sn grains with no directions [41].

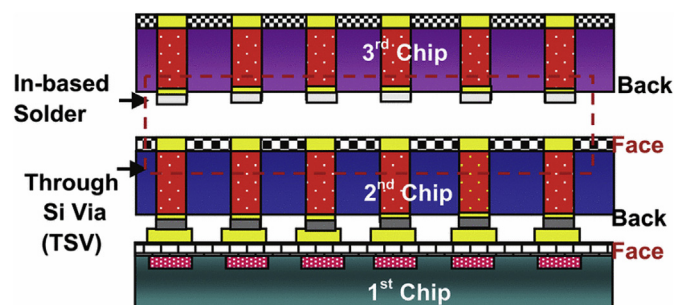


Fig. 7. Schematics of stacked dice fabricated by low temperature bonding [48].

without degradation. Warren [49] reported the first wafer-level vacuum packages created with Au–In TLP bonding (200 °C, 1 h, vacuum), after the transformation of the In layer, the melting temperature of the joints is raised from the melting point of the In layer (156 °C) to the melting point of the intermetallic compound (540.7 °C). Zhang [50] found that AuIn₂ can be formed during Au–Sn TLP bonding (180 °C, 1 MPa), the kinetics of AuIn₂ phase formation is diffusion controlled. It is worth mentioning that all the In was transformed into Au₁₀In₃ and Au₉In₄ were also identified in addition to the majority AuIn₂.

2.5. Cu–Ga bonding

An attempt has been made by Lin [51] to evaluate Ga-based Cu-to-Cu interconnection by transient liquid-phase (TLP) bonding, for the Cu/Ga/Cu sandwich-type couples, thin Ga layers with thickness 10 μm, 30 μm, and 50 μm were placed between two Cu substrates and annealed at 160 °C under 10^{−5} bar vacuum. At the Cu/Ga/Cu interface, CuGa₂ and Cu₉Ga₄ IMCs were formed at 160 °C, 200 °C, 220 °C, and 240 °C, while only Cu₉Ga₄ was formed in couples reacted at 280 °C and 300 °C. Sandwich-type Cu/Ga/Cu couples reacted at 160 °C solidified isothermally and formed Cu/Cu₉Ga₄/CuGa₂/Cu₉Ga₄/Cu, but the cracks were observed in the CuGa₂ phase regions, Fig. 8 shows the cracks at the Cu/Ga/Cu solder joints with different Ga thickness. In order to improve the performance of bonded joints, polycrystalline or single-crystalline Cu and Pt under bump metallization (UBM) were considered in Cu–Ga–Cu TLP bonding [52], for Ga-to-Pt ratios ($n \geq 4$) at 300 °C, the Cu/Pt/Ga/Pt/Cu interface evolves to Cu/fcc centered cubic (fcc)/γ₁-Cu₉Ga₄/fcc/Cu, Cu/fcc/γ₁-Cu₉Ga₄ + Ga₇Pt₃/fcc/Cu, and finally Cu/fcc + Ga₇Pt₃/Cu structures. The desired ductile solid solution joint formed with discrete Ga₇Pt₃ precipitates. The formation of Ga₇Pt₃ phase can enhance the reliability of Cu–Ga–Cu bonded joints. The element Ga has a melting point of 29.78 °C [53], the Ga selected as an interconnection materials for TLP bonding in 3D IC is a good choice for low temperature bonding.

2.6. Cu–In bonding

The melting temperature of indium (In) is 156.6 °C [54], due to its low melting temperature, In was selected as bonded materials in 3D IC effectively. The Cu–In bonding at 260 °C and 360 °C was investigated by Tian [55]. After bonding at 260 °C, Cu₁₁In₉ phase firstly observed and then Cu₂In phase formed between Cu₁₁In₉ layer and Cu substrate, the fractures in bonded joints were found at Cu₁₁In₉ layers and the fracture mode was cleavage fracture. After bonding at 360 °C, Cu₂In phase firstly generated and then parts of Cu₂In grains transformed to Cu₇In₃ phase, with faster nucleation and growth rate, especially along the direction of grain boundary for Cu₂In phase [56]. The intergranular fractures were formed at the interface between Cu₂In layer and Cu₇In₃ layer while the cleavage fractures were found at Cu₇In₃ layer. In addition, the formation of high-quality Cu₂In can improve the reliability of bonded joints. After Cu–In bonding at 200 °C (300s), Lee [57] studied the reliability (high-temperature storage (HTS): 300 °C, thermal cycling (TC): 40 °C–125 °C) of bonded joints. After bonding, the microstructures of bonded joints are composed of Cu₉In₁₁ and Cu₇In₃, the bonded joints were fully converted to Cu₇In₃ during HTS testing, no crack or defect could be observed. After 500 cycles of TC testing, relatively large voids and micro-cracks were observed in the middle of bonded joints, which can be attributed to cyclic stress formed during TC testing. Due to the mismatch of CTE (coefficients of thermal expansion) of different phases in joints [58], the cyclic stress will arise in the bonded joints, which can induce the formation of defects.

2.7. Ni–Sn bonding

In 3D IC, Ni–Sn TLP bonding was also an effective processing, which was proposed by many researchers. Yu [59] reported the Ni–Sn TLP bonding, Ni₃Sn₄ is formed at a bonding temperature of 250 °C, which can provide a temperature resistance joints higher than 600 °C, the formation energy of Ni₃Sn₄ was calculated to be

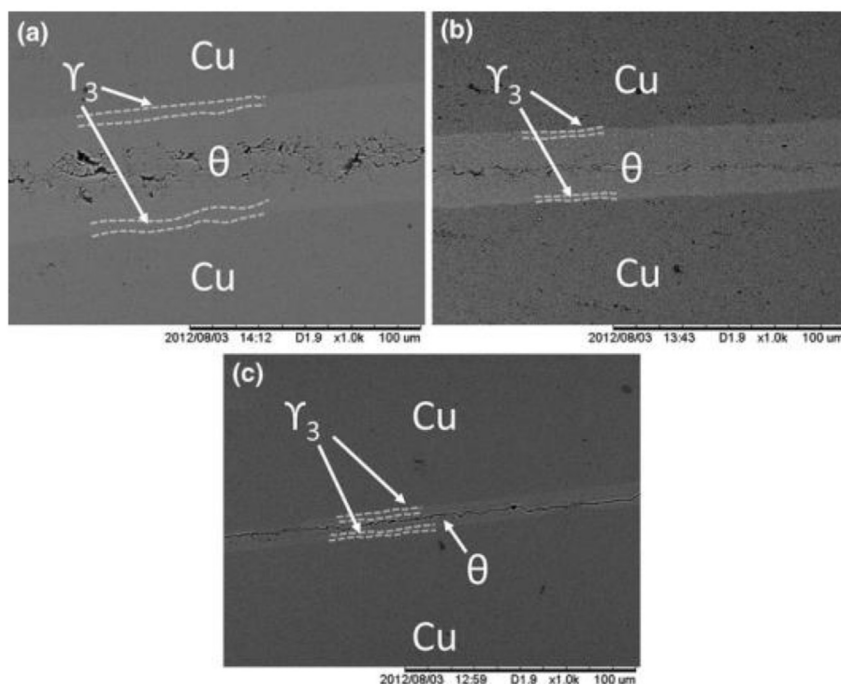


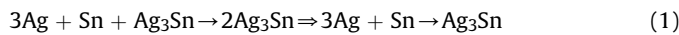
Fig. 8. BEIs of Cu/Ga/Cu couples with (a) 50 μm, (b) 30 μm, (c) 10 μm thick Ga layers reacted at 160 °C for 96 h [51].

23.15 kJ/mol. Lee [17] shows the Ni–Sn TLP bonding at 300 °C, electroless Ni(P) layer with 5 µm thick and contained approximately 15 at.% P, the microstructures of Ni–Sn bonded joints was shown in Fig. 9. Needle-type Ni_3Sn_4 phases at both the interfaces with 4 min bonding were observed, as shown in Fig. 9. Ni_3P phases were also found between Ni_3Sn_4 and electroless Ni(P) layer. With the increase of bonding time, Ni_3Sn_4 and Ni_3P all grew obviously. When the TLP bonding time was 2 h, bonded joints were completely transformed into the Ni_3Sn_4 phases, Ni(P) layer was also completely converted into Ni_3P layer, and some voids can be found in Ni_3P layer, in addition ternary Ni_2SnP layer was also observed between the Ni_3Sn_4 and Ni_3P layer. However, Li [60] found the void formation in Ni_3Sn_4 phases during the reaction between Ni and Sn. The temperature parameters can influence the interdiffusion of elements, which can determine the void formation.

In order to improve the property of Ni–Sn bonding, Hsu [61] selected Ni/Sn–2.5Ag/Ni bonded samples (295 °C, 30s) to simulate the microbumps in three-dimensional packaging. Annealing at 100 °C, 125 °C, and 150 °C for 100 h, 250 h, 250 h, 750 h, and 1000 h. After bonding, Ni_3Sn_4 phases formed at both sides of the bonded joints with Ag_3Sn phases randomly distributed in Sn solder. After thermal treatment Ni_3Sn_4 came into contact and eventually occupied the entire joint, Ag_3Sn particles pinned at the center of the bonded joints. However, serious cracks and defects were observed in the annealed samples. The growth rate constants of Ni_3Sn_4 at 100 °C, 125 °C, and 150 °C were 1.61×10^{-17} , 8.61×10^{-16} , and 1.10×10^{-14} , the activation energy associated with Ni_3Sn_4 growth was 171.8 kJ/mol, discrepancies among the activation energies calculated by different researchers can be attributed to differences in experimental parameters and analytical approaches. The Feng [62] reported Ni/Ni–Sn/Ni bonding, Ni and Sn mixed powder with alcohol were printed between Ni plates for bonding (300 °C, 340 °C, 0.1 MPa). After holding for 240 min at 340 °C, the bonding layer is composed of Ni_3Sn_4 and residual fine Ni particles with a small amount of Ni_3Sn_2 , which has a heat-resistant temperature higher than 790 °C. But for 3D IC, 340 °C is so high for the chip structure can not able to ensure the thermal can deform significantly.

2.8. Ag–Sn bonding

Ag–Sn TLP bonding (300 °C, 350 °C) was attempted by Lis [63], scallop-like Ag_3Sn phase can be formed between Ag and Sn firstly, with the time goes by, both Ag_3Sn growth front lines meet and leave behind entrapped Sn islands in the center of the joint which are isothermally transformed into Ag_3Sn . Equation (1) shows the reactions from incomplete to complete Ag_3Sn transformation:



When mass conservation is considered, the volume difference

ΔV between Ag_3Sn and base materials can be obtained from

$$\Delta V = 1 - \frac{1M(\text{Ag}_3\text{Sn})/\rho(\text{Ag}_3\text{Sn})}{3M(\text{Ag})/\rho(\text{Ag}) + 1M(\text{Sn})/\rho(\text{Sn})} \quad (2)$$

According to Equation (2), volume contraction of approximately 9 vol% can be found during the transformation process, the probability of shrinkage porosity is expected to increase when the remaining Sn islands are large. Under different processing temperatures, Ag_3Sn phase will represent different morphologies, when the temperature is so high, Sn islands can be observed in the matrix, and the sizes can be increase obviously, which induced the formation of pores. Li [64] also found the pores formed with in the Sn remaining, parts samples mainly consisted of Ag_3Sn phase, together with a few pores ranges from 2 to 25 µm in size. In service, the pores can provide the weak site for crack initiation to failure. Padilla [65] reported that cracks initiated at the two large pores and propagated along the interface based on finite element simulation, indicating the influence of pore size on failure of the joint.

3. Thermo-compression bonding

Thermo-compression bonding represents a chip or wafer metal diffusion bonding technique, is also referred as solid-state bonding [66]. The bonding occurs between metals interface with heat and pressure, under this condition, the elements diffusion may happen between two metals interfaces, the atomic interaction of interfaces varies obviously with the changes of bonding parameters. Moreover, the surface oxidation will reduce the reliability of bonded joints, so how to protect the metals interface become an important research topic to ensure low temperature thermal compression bonding in 3D IC.

3.1. Cu–Cu bonding

Cu metals often were selected as bonding materials due to its excellent electrical and thermal conductivity. Cu–Cu thermal-compression bonding was used effectively in 3D IC, and investigated by Tang [67], thermal compression differs from surface activation in that it uses a sufficiently high bonding force to ensure contact between wafer surfaces at 400 °C or lower and completes the interdiffusion of Cu atoms. Fig. 10 shows the microstructures of Cu–Cu bonded layers, according to the SEM and TEM figures, interdiffusion of both Cu layers occurred during initial bonding, jagged Cu–Cu interface indicated that both bonding time and supplied energy were insufficient to complete any grain growth of the bonded joints was shown in Fig. 10 (b). After 400 °C for 30min followed by nitrogen anneal at 400 °C for 30min, the distinguishable interface eventually vanishes as both Cu films homogeneously merge during the final phase. In general, the Cu–Cu bonding

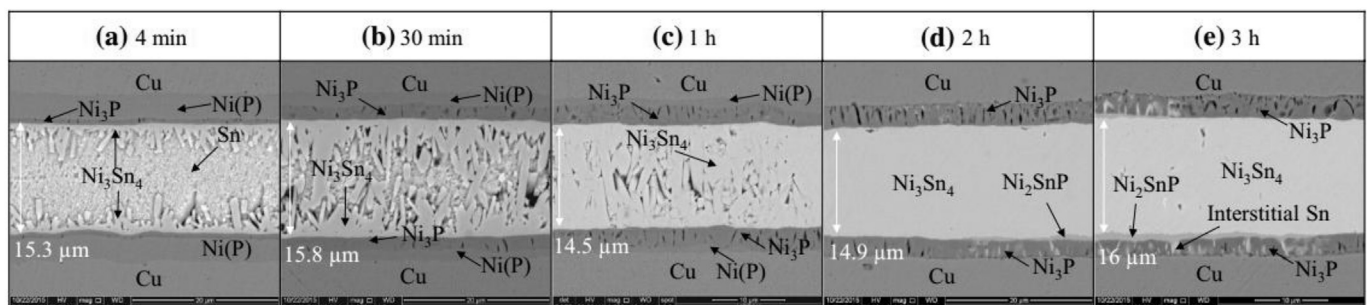


Fig. 9. SEM of Cu–Sn and Ni–Sn bonding [17].

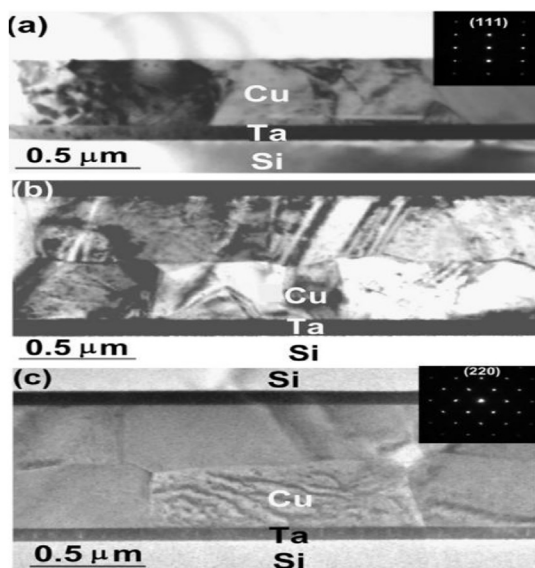


Fig. 10. Microstructures of Cu–Cu bonded joints (a) before bonding, (b) after 400 °C bonding for 30 min, and (c) after 400 °C bonding for 30 min followed by nitrogen anneal at 400 °C for 30 min [67].

temperature needs to be higher than 350 °C, and the bonding time larger than 30 min is also necessary [68]. Chen [69] described the relationship between reliability of bonded joints and bonding parameters (bonding temperature, bonding time, annealing time) as shown in Fig. 11, the bonding condition can be either 400 °C for 30 min followed by annealing at 400 °C for 30 min or bonded at 350 °C for 30 min followed by annealing at 350 °C for 60 min, the microstructures of bonded joints showed grain structure, the bonded joints represents excellent reliability, when the bonding temperature of Cu–Cu is lower than 350 °C, the defects can be observed obviously. Void phenomena in Cu–Cu bonded joints was studied by Gondcharton [70] in the temperature range (300 °C–400 °C). He demonstrated that voiding phenomena was related to a stress driven vacancy diffusion very comparable to standard metallurgical creep mechanisms.

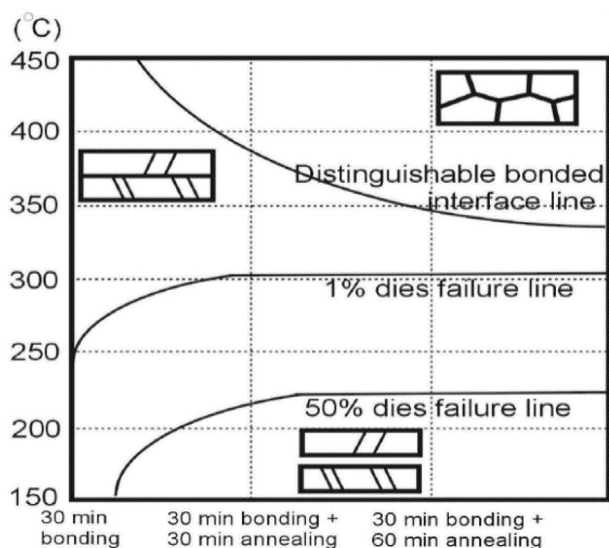


Fig. 11. Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [69].

The highly sinterable Cu nanoparticle paste was selected to be used in Cu–Cu bonding by Li [1], after sintering at the temperature from 200 °C to 300 °C for 60 min, it is found that the well-sintered nanoparticle paste presents good fluidity and large area of melting at 300 °C. The shear strength of bonded joints is 31.8 after bonding, after the isothermal aging test, the shear strength of the Cu–Cu joint shows a slight change, rising to 32.25 MPa. The microstructure of bonded joints was studied, due to the excellent flowability of the nanoparticle paste at the sintering temperature of 300 °C under the bonding pressure, the bonded joints shows few defects. From the microstructure, the sinterable Cu nanoparticle paste achieves a high efficiency of surface diffusion with Cu substrate, the join ability is so excellent. Moreover, the microstructure of the Cu–Cu bonding interface shows little changes after the isothermal aging test. The application of Cu nanoparticles can improve the property of bonded joints. Another paper [71] reported that the highest shear strength of 35.48 MPa was achieved at 400 °C and the bonding pressure of 40 MPa. Zou [72] researched the effect of different sizes of Cu nanoparticles (20–100 nm) on the shear strength of Cu–Cu joints, the bonding strength of joints over 15 MPa was achieved even at a lower bonding temperature of 250 °C and pressure of 4 MPa. Cu nanoparticles were selected effectively as an interconnection materials in Cu–Cu bonding, but the defects can be observed obviously in bonded joints, which can degrade the reliability of Cu–Cu bonded joints in service, so how to reduce the defects in bonded joints may be the important aspect of Cu–Cu bonding with Cu nanoparticles paste.

Tan [73] proposed to use self-assembled monolayer (SAM) of alkane-thiol with the aim to protect the Cu surface against excessive oxidation in Cu–Cu thermo-compression bonding. The bonding parameters were 250 °C and 250 kPa for 1 h in vacuum (~1e-4 mBar), in the bonded joints, substantial out-of-plane grain growth across the bonding interface has taken place and the original bonding interface has disappeared. It was indicated that Cu grains extended beyond the original bonding interface and wiggling grain boundaries were formed. Meanwhile, the shear strength of bonded joints is enhanced to the range of 54.0–65.8 MPa from the control value with no SAM treatment of 8.6–11.1 MPa. SAM treatment on Cu surface provides protection against oxidation and improves the bonding quality, the method does not require mechanical desorption hence it is gentle for 3D integration [74]. Argon plasma treatment on Cu surface for Cu–Cu bonding can also improve the bonding quality, the Cu–Cu thermo-compression bonding was performed at 300 °C under 2 MPa for 1 h right after the Ar plasma treatment [75].

The Cu–Cu bonding was conducted at 150 °C for 30 min with 1.7 MPa pressure, before bonding the native Cu oxide was removed with a combination of citric acid and forming gas treatment [76], finally post-bond annealing (no force) was performed at a fixed temperature of 200 °C for bonding time of 1, 6 and 24 h, respectively. The voids can be observed in the SEM figures as shown in Fig. 12, it is found that with the increase of annealing time, the amounts and the size of voids increase obviously. In the whole structure, the coefficient of thermal expansion (CTE) mismatch of different materials causes stress, which can inducing the size increase of voids. After Cu–Cu bonding (vacuum ambient, 250 °C, 300 °C, 350 °C, 5500 N pressure) excellent helium leak rate can be demonstrated, which is smaller than the reject limit defined by MIL-STD-883E standard (method 1014.10), meanwhile excellent mechanical and hermetic bonds at low temperature (≤ 300 °C) can be found [77].

3.2. Cu–Sn bonding

Cu–Sn thermo-compression bonding can also be used in 3D IC,

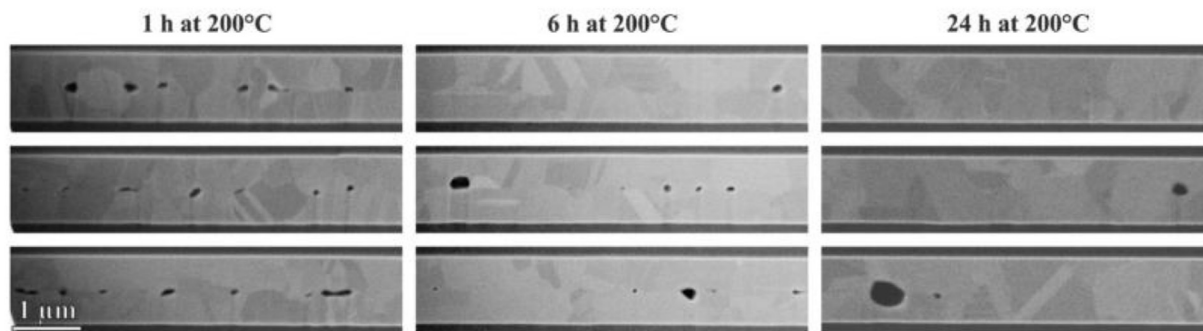


Fig. 12. Typical cross-sections of Cu–Cu wafer pairs bonded at 175 °C for 30 min after subsequent 1, 6 and 24 h post-bond annealing at 200 °C [76].

the bonding temperature is below the Cu–Sn eutectic temperature (227 °C), during the bonding, the reaction between Cu and Sn can occur to form the Cu_6Sn_5 and Cu_3Sn intermetallic compounds, intermetallic compounds types are same with the phases in Cu–Sn transient liquid phase bonding. The last determinations are all to obtain high-temperature Cu_3Sn bonded joints [78]. The high temperature stability was verified for Cu–Sn bonding based on shear testing. Cu–Sn bonding at 207 °C and 100 N/bumps was carried out by Pun [79], to investigate the solid-state growth kinetics of intermetallic compounds in Cu pillar solder flip chip with ENEPIG surface finish under isothermal aging, the types of IMCs formation, it was found growth rate, and reliability of Cu pillar joint strongly depended on bonding temperature, Au and Pd thicknesses, and solder volume. A novel pretreatment of plasma combined self-assembled monolayer (PcSAM) was proposed to improve surface properties of electroplated Cu for low temperature Cu–Sn thermo-compression bonding in 3D integration [80], the bonding was performed with pressure of 15 MPa at 200 °C for 30 min under vacuum of 10–3 Pa in wafer bonder, the annealed temperature is 200 °C for 60 min under N_2 atmosphere. The Cu–Sn bonding interface exhibited a defect-free interconnection, and bonding strength has reached as high as 68.7 MPa. Cu bumps are easily oxidized to form a thin copper oxide, which would reduce the surface activity and impede Cu–Sn diffusion, the pretreatment of Cu is to remove the oxygen contained layer, smoothen the surface, and suppress the oxygen adsorption [81].

4. Surface activated bonding

The surface activated bonding (SAB) process is a solid-state bonding process in which two or more smooth surfaces are cleaned by using either an argon fast atom beam (Ar-FAB), an Ar ion beam, or a radio frequency (rf) plasma in an ultrahigh vacuum (UHV) followed by contact, which results in strong adhesion between thematized surfaces [82–85]. The driving forces of the SAB process are the integration potential at room or low temperature, which eliminates thermal mismatch problems, and the production of electrically and microstructurally useful interfaces with bonding strengths comparable to bulk materials [86,87]. Therefore, the SAB process can be a packaging solution for three-dimensional integration of multifunctional materials to achieve high density and multifunctional devices at low total packaging costs [88–90]. Moreover, Surface activated bonding in an ultrahigh vacuum at room temperature has many advantages as a low damage bonding method [91].

4.1. Wafer level direct bonding

In 1996, Takagi [92] reported the surface activated bonding of

silicon wafers directly at room temperature with surface activated by argon atom beam etching and brought into contact in vacuum. The surfaces of the specimens were activated by sputter etching with argon fast atom beam (FAB 110, IonTech Ltd., England). Etching conditions were 1.5 kV applied voltage, 20 mA plasma current for each gun. From the Auger electron spectroscopy, 5 min etching was enough to remove surface contaminants such as adsorbed gas, hydrocarbon, and natural oxide and created pure silicon surface. After the etching, two specimens were brought into contact with the pushing pressure of 1 MPa to achieve bonding. For the bonded joints, no voids can be found, which can enhance the bonding strength. Chung [93] showed room temperature GaAs–Si and InP–Si wafer direct bonding by the surface activated bonding method, the surfaces to be bonded are sputter-cleaned and activated by argon fast atom beam (FAB) bombardment and then brought into contact with each other in an ultrahigh vacuum. Takagi [94] used surface activated by Ar beam sputter etching to bond Si wafer with LiNbO_3 , LiTaO_3 , $\text{Gd}_3\text{Ga}_5\text{O}_{12}$, the mechanical testing demonstrated that the structure show sufficient strength after bonding, and found that the SAB bonding is suitable for the bonding of dissimilar material combinations with large thermal expansion mismatches. In addition, four-inches Si wafers can be bonded in vacuum after Ar beam sputter etching [95], the samples bonded at room temperature are so strong that bulk fracture is observed after tensile test, both heat treatment and applying pressure are not required in the bonding. The SAB bonding can also be utilized in fabrication of GaInP/GaAs/Si solar cells [96], the argon fast atom beam treatment of the surfaces before wafer bonding leads to a 4–5-nm-thin amorphous layer which causes voltage losses under high current densities.

4.2. Au–Sn bonding

Wang [97] developed a low-temperature bonding process of 30-mm-pitch Au–Sn microbumps in ambient air by the surface activated bonding (SAB) method. The structure was shown in Fig. 13. The 4908 electroplated Au pads and Au–Sn bumps were prepared on under bump metallurgy (UBM) of the Si chips and substrates respectively. With a SAB flip-chip bonder, the activate sample surface was treated under 7.5 Pa pressure with an Ar plasma background, during bonding (30s), specific bonding temperature (100, 150, or 200 °C) was selected. Based on optimization design, the bonding parameters are around 100 MPa at 100 °C, 50 MPa at 150 °C, and 25 MPa at 200 °C. The bond yield reaches 100%, and the bonding strength reaches more than 10 Mpa, it is found that the bonding pressure has no effect on bonding strength. Moreover, surface roughness is an important role in SAB to guarantee an enough contact area [98]. During bonding, the reaction between Au and Sn will happen. According to Au–Sn phase diagram [99], main

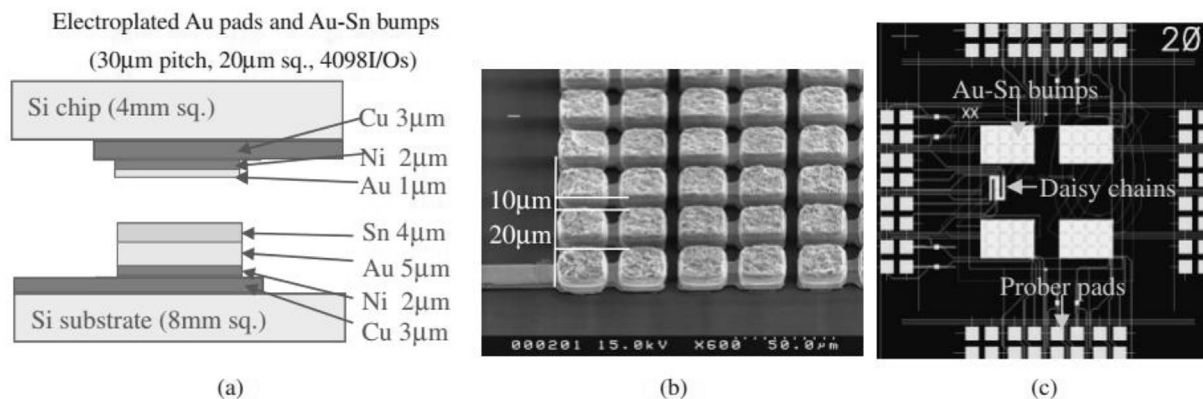


Fig. 13. (a) Structure of a bonding pair, (b) SEM image of Au–Sn bumps, and (c) layout of the substrate [98].

three different phases of Au–Sn can be found, namely AuSn, AuSn₂, and AuSn₄. At 200 °C the interdiffusion between Au and Sn is stronger, Au₅Sn and AuSn phases were observed on the Au pad, AuSn₂ and AuSn₄ were found on the Sn side. AuSn, AuSn₂, and AuSn₄ appear around the bonded interfaces at 100 and 150 °C, no Au₅Sn was detected. Based on aging (125 °C, 200 °C, 18 h), the amounts of AuSn and Au₅Sn phase increase with the disappearance of AuSn₄ and AuSn₂ at 125 °C aging, only Au₅Sn phase remains after aging at 200 °C aging. Yamada [100] investigated the formation of intermetallic compound layers in Sn/Au/Sn diffusion couple during annealing at 160 °C, found that the grain boundary diffusion partially contributes to the rate-controlling process for the growth of the compound layers.

4.3. Cu–Cu bonding

In electronic industry, the use of Cu instead of Al is critical to reduce the RC delay, so the Cu–Cu bonding technology has become an important technique in 3D IC. The surface activated bonding (SAB) can ensure the Cu–Cu bonding at room temperature based on the Cu surface before bonding activated by a low energy Ar ion beam of 40–100 eV [101], the bonding was carried out under an ultrahigh vacuum condition. The tensile testing indicated that no fracture was observed in the Cu–Cu bonded joints, between Cu surfaces the excellent interconnection was found, which can be attributed to an attractive intermolecular force [102]. Ultrafine pitch bonding of Cu electrodes can also be conducted on surface activated bonding flip-chip bonder that enables the alignment of $\pm 1 \mu\text{m}$ in a high-vacuum condition [103], the bonding strength is larger than 50 MPa. The TEM observation showed that the interconnection was successfully obtained between Cu grains without visible void and the oxide layer at the interface [104]. The roughness of CMP-Cu is around several nm, then it means the contact problem is not the fatal problem of SAB of Cu [105].

4.4. Cu-adhesive hybrid bonding

In 3D IC, Cu/adhesive hybrid bonding is an attractive approach to form high-quality bonding joints because it can provide direct Cu–Cu vertical interconnects with improved thermal-mechanical stability compared to the direct Cu–Cu bonding. For the traditional Cu/adhesive hybrid bonding, as shown in Fig. 14(a) [106], the adhesive bonding and subsequent adhesive curing can happen firstly at below 250 °C, then the thermo-compression bonding was conducted at 350–400 °C, the temperature is much higher than that of adhesive/curing (≤ 250 °C, depending on the glass transition temperature T_g of the adhesives [107,108]), which may damage the

adhesive if it is not fully cured beforehand. In order to boost the bonding reliability, He investigated and demonstrated a “Cu-first” hybrid bonding technique by using hydrogen(H)-containing formic acid (HCOOH) vapor prebonding surface treatment for the first time, the bonding was done at below 200 °C with in a short time before adhesive curing, as shown in Fig. 14(b), the adhesive curing occurred at below 250 °C. The present technique can be useful to improve Cu/adhesive hybrid bonding at below 200 °C with small thermal stress, high throughput, and low cost.

4.5. Au–Au bonding

Because surface-activated bonding is based on the interatomic attraction forces on an atomically clean active surface, a strong bonded joint can be formed between the mating smooth surfaces when they are in close contact. Higurashi [109] report successful 3D integration of optical chips performed using Au–Au surface-activated bonding at a relatively low temperature of 150 °C. The clean active surfaces (Au) were prepared by irradiation of argon RF plasma (oscillation frequency: 13.56 MHz; RF power: 100 W; plasma pressure: 7.6 Pa). A glass substrate with the flip-chip-bonded photodiode (PD) chips was vertically stacked on a Si substrate with the bonded LD chip using low-temperature Au–Au SAB to realize high-density microsystems packaging. Based on this method, compact and thin optical microsensors were fabricated. Low-temperature bonding of laser diode chips on silicon substrates using plasma activation of Au films was conducted successfully [110], the organic contaminants on the Au surfaces of the samples are removed by an Ar-radio frequency (RF) plasma (oscillation frequency: 13.56 MHz, RF power: 100 W, plasma pressure: 7.6 Pa) in the pretreatment chamber, and etching rate for Au film is about 30 nm/min, then the bonding was carried out by contact for 30 s at lower temperature (< 250 °C) in ambient air.

5. Adhesive bonding

Adhesive bonding is an effectively method to carry out the 3D chip stacking using polymer, SU-8 and BCB (benzocyclobutene) are the most common material used for wafer level adhesive bonding in 3D integration and application [68]. The bonding represents favourable bonding strength excellent surface planarization property, high plasticity, and meets the low temperature requirement of 3D IC. In addition, comparing with TLP bonding, no intermetallic compounds formed at the interface, no stress can be concentrated in the adhesive joints, in service, the adhesive joints are not sensitive to the stress-strain. For the most polymer in adhesive bonding, limited temperature stability and limited long-term

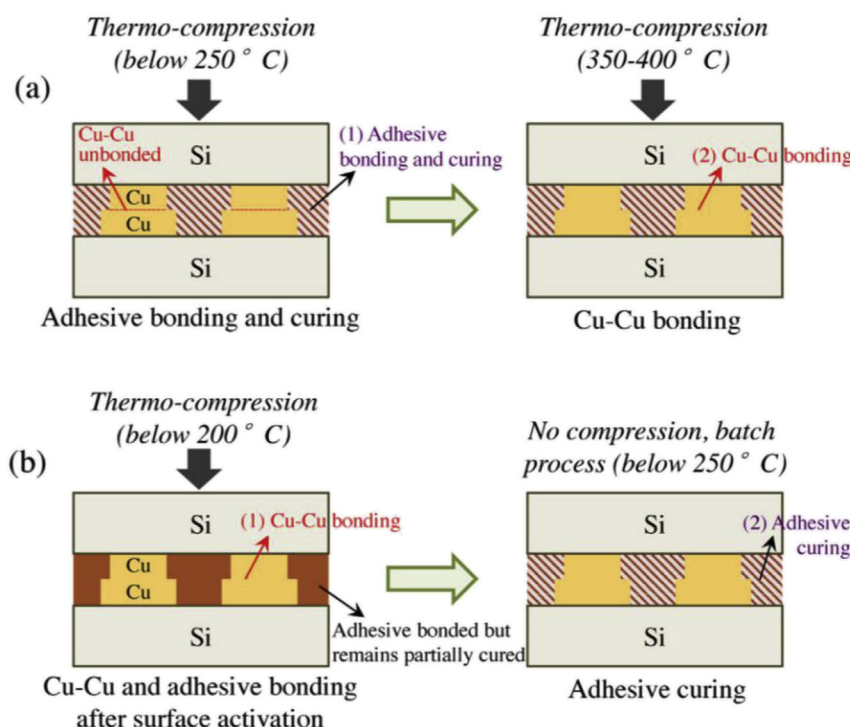


Fig. 14. Cu/adhesive hybrid bonding through (a) “adhesive-first” hybrid bonding and (b) “Cu-first” hybrid bonding investigated [106].

stability may be the disadvantages [111] to restrict the further extensive application.

BCB often is used as the intermediate bonding materials, which does not release significant amounts of byproducts during the curing process. Niklaus [112] investigated the low-temperature full wafer adhesive bonding, and systematically studied the influence of different bonding parameters and different polymer materials on void formation in a low-temperature adhesive bonding. It is found that the selection of adhesive is the most important factor to achieve void-free bonds. BCB was demonstrated to be the optimal adhesive material, which can conduct the bonding with 180 °C, and induce very strong, void-free bonded joint. The BCB can also be utilized in stacked solar cells (GaAs–InGaAs) within adhesive bonding [113]. A dual-junction, GaAs–InGaAs, MSSC has been demonstrated using a BCB adhesive layer with a measured PV conversion efficiency of 25.2% under 1-sun AM1.5G conditions, which can be further enhanced by thinning of the top cell substrate to reduce long wavelength absorption and optimization of the optical index matching properties of the ARC used between the top/bottom cells and intermediate adhesive. A thin layer of polydimethylsiloxane (PDMS) prepolymer coated on a glass slide used by Wu [114] in the construction of microfluidic chips, is transferred onto the embossed area surfaces of a patterned substrate. This coated substrate is brought into contact with a flat plate, and the two structures are permanently bonded to form a sealed fluidic system by thermo curing (60 °C for 30 min) the prepolymer.

Pan [115] used UV epoxy resin for the adhesive bonding of glass blanks and patterned plates at room temperature for glass microfluidic chip, there is no need to use a high-temperature thermal fusion process and therefore avoid damaging temperature-sensitive metals in a microchip. It is shown that the sealed glass blanks and patterned plates can be separated by the application of adequate heat. UV adhesive bonding technique for the rapid and low-cost bonding at room temperature has been developed and used effectively, the entire bonding process can be carried out at

room temperature in less than 30 min, involved only user-friendly laboratory operations, and provided a near 100% success rate [116,117]. The adhesive bonding process with Ordyl for 3D MEMS integration was investigated by Huesgen [118], the bonding temperatures are 80–120 °C before inserting the wafer stack. The bond pressure of 40–80 N cm² builds up immediately after transferring the wafers into the bond chamber and is maintained for 30 min.

In the manufacture of three-dimensional (3D) interconnected microchannels [119], 3D embedded microchannels are fabricated by a low temperature adhesive bonding of the SU-8 photo patterned thick films, the bonding temperatures are 100–120 °C. Based on the optimization of bonding parameters, a strong and void-free bond joint can be obtained effectively. Lima [120] developed sacrificial adhesive bonding, namely the adhesive layer was sacrificed in the bonding. Initially, an uncured SU-8 intermediate was used to seal two glass slides irreversibly as using adhesive bonding with SAB. Subsequently, an additional step removes the adhesive layer from the channels.

In addition, hybrid Au-adhesive bonding using planar adhesive structure for 3-D LSI was reported by Nimura [121], Fig. 15 plots the fabrication process of the planar adhesive structures, which will be used for hybrid bonding in the later step. Firstly, uncured and partially cured adhesive was formed on the chip and substrate, respectively. The hybrid bonding was carried out in three steps using a flip-chip bonding machine in ambient air. Fig. 16 shows the hybrid bonding process, no surface treatment was used in the bonding process. Firstly, the Au bumps were contacted in room ambient to prevent trapped adhesive after alignment by a charge-coupled device camera. Secondly, the uncured adhesive of the chip was glued to the partially cured adhesive of the substrate at 150 °C for 300 s. Lastly, Au–Au thermo-compression bonding was carried out at 250 °C for 500 s. Then, the samples bonded with adhesive were fully cured at 250 °C for 1 h, and the Au diffused at the Au–Au bonding interface simultaneously.

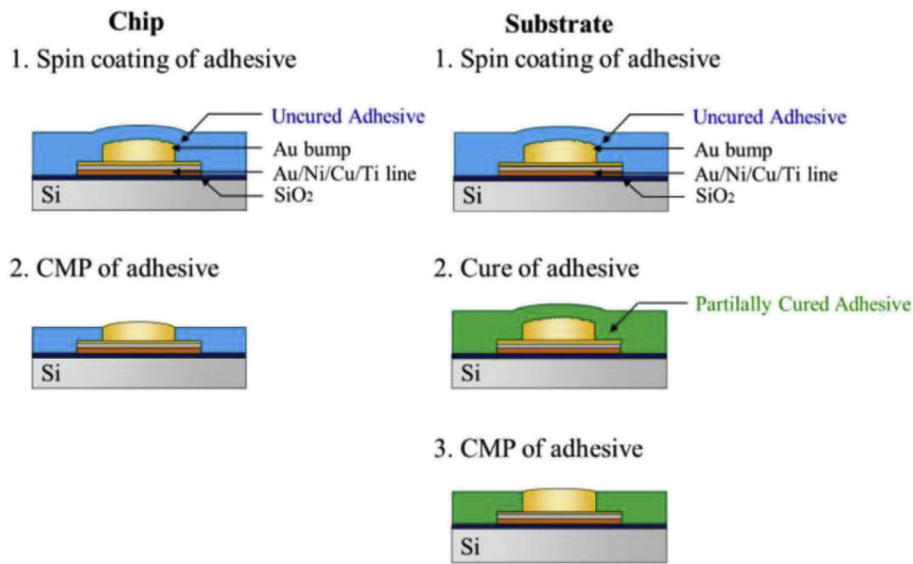


Fig. 15. Fabrication process of planar adhesive structure [121].

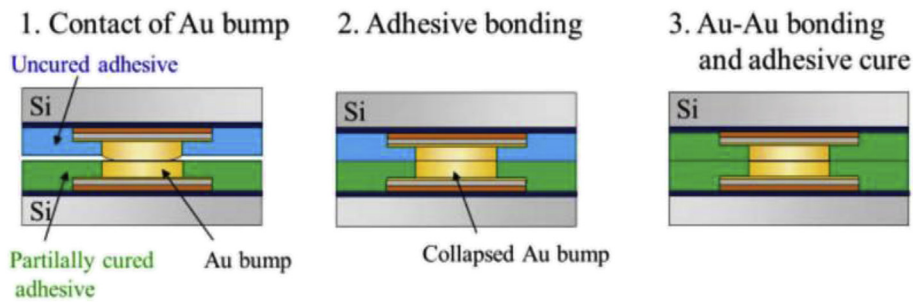


Fig. 16. Hybrid bonding process [121].

6. Ultrasonic bonding

Ultrasonic bonding was developed in mid-1960s, which was utilized to bond different materials to form joints with high strength and good electric/thermal conductivity. Even though the surface temperature rise up to 200–300°C due to the friction of two contacting metal surfaces, the heating process is localized and bonding time is very short [122]. Ultrasonic bonding is widely used for electronic packaging [123,124].

6.1. Metals ultrasonic bonding

Ultrasonic bonding approaches have been developed including lateral and vertical ultrasonic bonding setups with three sets of material bonding systems: In-to-Au, Al-to-Al, and plastics-to-plastic [125] for hermetic sealing of MEMS sealing and packaging. All parameters used in the experiments are summarized in Table 1

using the lateral setup, comparing with vertical ultrasonic bonding, it is found that the lateral vibration setup gives better bonding results for MEMS packaging and sealing applications, however, vertical vibration setup can induce local energy concentration and will be better applicable for specific bonding and sealing applications. Li [126] analyzed the microstructure of Au/Al ultrasonic bonding, the velocity of ultrasonic vibration at the wedge capillary was determined with a PSV-400-M2 High Frequency (1.5 MHz) Laser Doppler Vibrometer, atomic diffusion in vertical sections of specimens prepared by an ultrasonic bonding process was studied by the use of TEM, complemented by EDS analyses. The thickness of the atomic inter-diffusion layer was measured as about 500 nm for an Au/Al joint, in which Au₄Al was formed, based on pull-testing, no fracture can be observed in joint interface. The results indicated that ultrasonic irradiation of materials alters the defect structure by stimulating significant increases in the dislocation density. The rapid dislocation channel mechanism of the ultrasonic bonding

Table 1
Bonding parameters used in the experiments [125].

Parameters	In/Au	Al/Al	Polymeric bonding (cellulose acetate)
Power supply output	20–25 Watts	30–50 Watts	20 Watts
Bonding time	0.8–1.8 s	2.5–5.0 s	2.0 s
Pressure	9.20–15.4 MPa	20.8–40.1 MPa	1.03–2.58 MPa
Vibration amplitude	0.8–1.5 μm	0.8–1.5 μm	N/A
Total bonding area on one chip	1.59–2.12 mm ²	1.59–2.12 mm ²	1.90 mm ²

process happens when the temperature is relatively low [127].

Au bump interconnection with ultrasonic flip-chip bonding in 20 μm pitch was carried out by Tanida [128], the parameters of ultrasonic bonding is 300 ms in 50 kHz, the temperature of both the metal tool and metal stage were set at 150 °C. The lower limit bonding conditions were confirmed to be a bonding force of 20 N and an amplitude of 3 mm, the bonding accuracy achieved was within 2 mm, the electrical interface resistance was stable about 0.57, and no damage around the interconnection structure was observed. In addition, the results above indicate that the atomic-level solid phase bonding without solid phase diffusion is the dominant bonding mechanism of the Au–Au interface by the ultrasonic flip-chip bonding process. Ultrasonic gold ball bonding was performed by Qi [129], the transducer frequency was 138 kHz and bonding time was fixed at 5 ms, bonding force was fixed at 200 mN and the bonding power varied from 40 to 480 mW to investigate the effect of bonding power. With the increase of bonding power, the non-slip and consequently unbonded central area can be reduced obviously. When the bonding power is too high, undergo plastic deformation can be observed in the bump, the ultrasonic power transferred to the interface will decrease significantly and the bonded area will not increase with bonding power increase in the higher range.

Room temperature Cu–Cu bonding was carried out by using ultrasonic vibration together with compression force to the bonding of a cone-shaped bump by Qiu [130]. The ultrasonic bonding was carried out at room temperature with the application of a compression force 1 gf/bump (121 N/chip) in 1.5s, the ultrasonic frequency was 48.5 kHz, it is successful that the Cu–Cu micro-joining can be performed. The mechanical testing showed that the bonding strength increases with vibration amplitude and depends on the thickness of the counter electrode made of Cu, which can meet the requirement from the application. Moreover, Arai [131] studied the effect of ultrasonic vibration energy on the Cu–Cu bonding, the Cu bumps with 20 μm height were bonded with sufficient strength as much as the reference strength of Cu bump before bonding, the Cu bumps with 40 μm height were bonded with poor strength compared with reference strength, Cu bumps with 5 μm height were not bonded successfully.

6.2. Solder ultrasonic bonding

In 3D IC structure, the ultrasonic bonding can be used in chip stacking with solders. Li [132] selected ultrasonic bonding to bond Ti/Ni/Cu wafer (4s, 0.6 MPa) using Sn interlayer, after bonding, high-melting-point Cu_3Sn intermetallic compound can be observed in the bonded joints, the shear strength is 635.8 MPa, the electrical resistivity is 67.3 $\mu\Omega\text{cm}$. During bonding, the ultrasonic vibration can enhance the diffusion of Cu from the metallization in to the molten Sn, which can induce the rapid formation of this Cu/Cu₃Sn/Cu joint. Ultrasonic vibration served as a heating source to rapidly melt the solder interlayer and subsequent sonochemical effects induced by acoustic cavitation at the interface between the liquid Sn and the solid Cu dramatically accelerate the melting diffusion kinetics [133].

The rapid transient liquid phase bonding process on Ag/Sn/Ag system is achieved in air by the assistance of ultrasonic, which has great potential to be applied to high-temperature power devices packaging [134]. Fig. 17(a)–(c) show the microstructures of the joints bonded at 250 °C for various time with 300 W ultrasonic. After ultrasonic bonding with 2s, scallop-like Ag_3Sn interfacial layer can be found between Ag and Sn, and large amounts of Sn exist in the matrix, only small amounts of Sn was reacted with Ag, when the bonding time further increase to 5s, the Ag_3Sn layers on both sides impinged on each other, leading to the isolation of residual Sn into

separate areas. When the bonding time is 15s, the Sn layer was completely reacted with Ag to form Ag_3Sn intermetallic compounds joint. Fig. 17(d)–(f) show the microstructures of the joints bonded at different temperatures for 15 s with 300 W ultrasonic. It is found that with 15s bonding and different temperature (280 °C, 310 °C, 340 °C) full Ag_3Sn IMC joints could be obtained, but the IMC thickness can be enhanced with the increase of temperature. However, wholly not exceeded the theoretical thickness of the Ag_3Sn layer (about 58 nm), which was calculated by the expression as follow:

$$t_{\text{Ag}_3\text{Sn}} = \frac{\rho_{\text{Sn}}}{\eta \rho_{\text{Ag}_3\text{Sn}}} t_{\text{Sn}}$$

where ρ_{Sn} (7.28 g/cm³) and $\rho_{\text{Ag}_3\text{Sn}}$ (9.39 g/cm³) are the densities of Sn and Ag_3Sn , η (26.83%) is the mass proportion of Sn in Ag_3Sn , and t_{Sn} (20 nm) is the thickness of Sn foil.

Homogeneous (Cu, Ni)₆Sn₅ intermetallic compound joints rapidly formed in asymmetrical Ni/Sn/Cu system using ultrasound-induced transient liquid phase soldering process was investigated by Li [135], comparing with traditional TLP bonding, the ultrasound vibration (bonding parameters: 260 °C, 20 kHz, 0.2 MPa and 400 W) can enhance the formation of (Cu, Ni)₆Sn₅. For the samples bonded by ultrasound-induced TLP soldering process, only exhibited uniform rounded shape grain morphology of (Cu, Ni)₆Sn₅ IMCs can be found, and the Ni concentration gradient across the intermetallic joint was remarkably narrowed. Under the sonochemical effects of ultrasonic waves, the rapid non-interfacial growth (Cu, Ni)₆Sn₅ IMCs can induce the homogenization microstructure. For the mechanical testing, the shear strengths of the joints bonded by the traditional reflow and ultrasound-induced TLP soldering processes were 49.8 MPa and 61.6 MPa, respectively. It can be found that the shear strength of joints bonded by ultrasound-induced TLP soldering is so higher than that by traditional reflow soldering. For the microstructure figures as shown in Fig. 18, the cracks can be found in the joints, which can be attributed to the mismatch between two grain areas with different elastic moduli, which would induce stress concentration and stress discontinuities at the interface during shear testing [132], this phenomenon can result in that the fracture easily occurred along the boundary-line between the needlelike and coarse rounded grain areas as presented in Fig. 18(a). However, for the joints bonded by the ultrasound-induced TLP joints as shown in Fig. 18(b), the homogenized (Cu, Ni)₆Sn₅ grains can be observed in the matrix, no such boundary-line existed as the fast propagation path of cracks.

6.3. ACFs ultrasonic bonding

Ultrasonic bonding is an attractive alternative to the ACF bonding process, as it is generally known that polymer materials generate a large loss modulus [136,137], which leads to energy loss in the form of heat dissipation. Lee [138] investigated the curing and bonding behaviors of ACFs by ultrasonic vibration using a 40 kHz ultrasonic bonder with longitudinal vibration, due to rapidly reaching a high temperature, ultrasonic bonding can induce the rapid curing of the ACFs in the ACF layer, i.e., above 300 °C, after 2 s. Ultrasonic bonding of ACF can significantly reduce ACF bonding time to several seconds, and also makes bonding at room ambient possible compared with T/C bonding which requires tens of seconds for bonding time and a bonding temperature of more than 180 °C.

The effects of ultrasonic bonding process parameters on the degree of cure and bond strength of polymer-based anisotropic conductive film joints are discussed by Lin [139], bonding time and ultrasonic power can enhance the degree of cure of ACF material

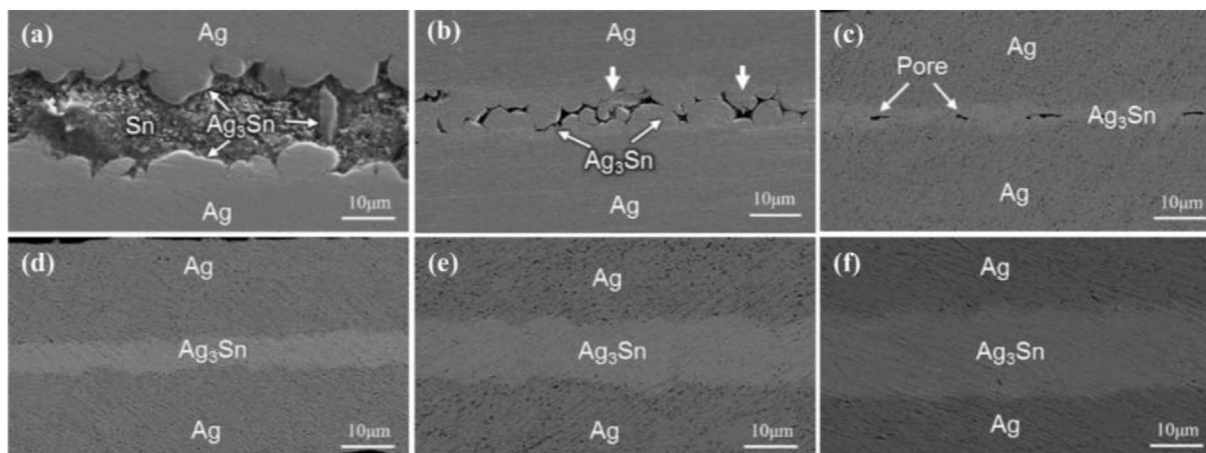


Fig. 17. Cross-sectional microstructures of the joint bonded at different temperature for various time with 300 W ultrasonic and 0.5 MPa bonding pressure: 250 °C for (a) 2 s, (b) 5 s, and (c) 15 s; (d) 280 °C, (e) 310 °C, and (f) 340 °C for 15 s [134].

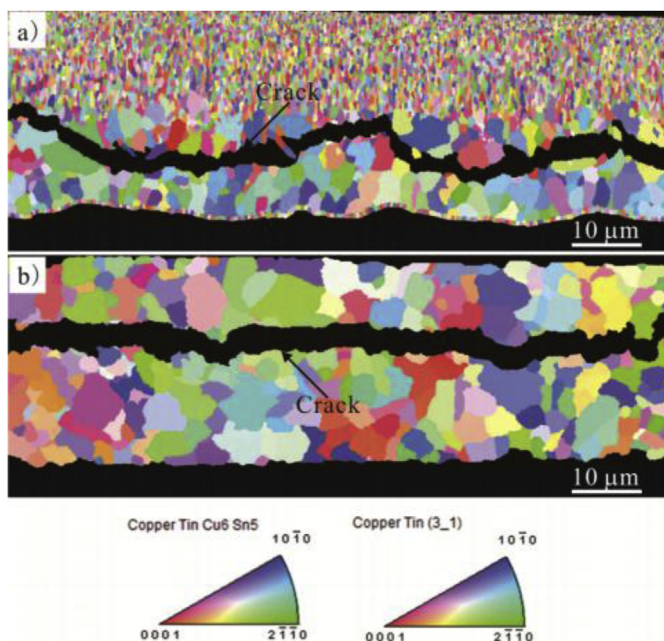


Fig. 18. EBSD analysis with grain mappings of the fracture samples of the joints formed by (a) traditional reflux TLP soldering process; and (b) ultrasound-induced TLP soldering process [135].

and ACF bond strength obviously, but the bond strength of the ACF joints rapidly decreases when the ultrasonic power is continuously increased, while there was negligible effect of bonding force, which can be attributed to. Based on optimization design, the parameters is 3s for bonding time, 3.5 W for ultrasonic power. Jang [140] reported that lower values of bonding pressure and temperature than recommended by the ACF specification can be adopted for reliable bonding, which proves the feasibility of the ultrasonic bonding technique.

7. Issues of low temperature bonding in 3D IC

3D IC packaging consists of two or more conventional components stacked in the vertical direction [141], 3D interconnection solutions and options continue to dominate the electronics manufacturing industry's attention over the last few years and

interest in the topic has been accelerating [142]. Several low temperature bonding methods can realize the interconnection in 3D IC, but there are some issues need to be studied further as follows: (1) Thermomigration: In 3D IC bonding technology, i.e., TLP bonding, the vertical interconnection consists of through-Si-vias (TSV) and micro solder bumps [143]. The diameter of micro-bump is around 10 mm, the joule heating is expected to be the most serious issue in 3D IC, heat flux must be conducted away by temperature gradient. If we import 1 °C difference across a micro-bump, the temperature gradient will be 1000 °C/cm, which can induce thermomigration at the device work temperature. Therefore, thermomigration will become a very serious reliability problem in 3D IC technology, for different low temperature bonding in 3D IC, the thermomigration should be investigated systematically. (2) Electromigration: in 3D bonding with solder bumps, the electromigration induced by diffusion of Cu atoms into Sn layers can occur in service [144], which can degrade the reliability of bonded joints, how to enhance the electromigration-resistance property may be the important aspect in 3D IC. Xiao [146] suggested that Ni layer electroplating between Sn and Cu layer can mitigate the diffusion of elements, but for 3D IC the complete IMC bonded joints is the main objects to meet the requirement of low temperature bonding and high-temperature work, mitigation of elements diffusion can not improve the electromigration-resistance performance of IMC bonded joints, but for Micro C4 solder interconnection in 3D chip stacking, the method may be an effective way to enhance the electromigration-resistance because of the existence of Sn and only IMC layer in solder joints. (3) Fatigue: after low temperature bonding, especially for solder bump, the intermetallic compounds joints can be formed, due to the brittle of intermetallic compounds, the crack induced by stress can be initiated and propagated in service [147], which can result the fatigue failure of the 3D IC.

8. Conclusions

To conclude this review, we note that different low temperature bonding methods have been developed to chips stacking in 3D IC. Materials, processing and reliability will be extremely important, their effects on the 3D IC structure were addressed in detail. However, many low temperature bonding methods were restricted to academic research, little work was done about the thermomigration, electromigration and fatigue, until the three issues of different bonding methods were investigated systematically. In addition, in view of the very rapid market growth in consumer

electronic products, the low temperature bonding may need further study in 3D IC.

Acknowledgements

The present work was carried out with the support of the Natural Science Foundation of China (51475220), the Qing Lan Project, the China Postdoctoral Science Foundation funded project (2016M591464), Six talent peaks project in Jiangsu Province(XCL-022), International Cooperation Project (2015DFA50470), Major State Research Development Program of China (2017YFB0305500), and Doctor Talent Project of Jiangsu Normal University(14XLR025).

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