Materials for heterogeneous integration

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Emerging artificial intelligence (AI) applications require dense connectivity between integrated circuit (IC) chips to enable high-speed computations. Heterogeneous integration (HI) using advanced packaging is being viewed as a critical enabling technology for supporting AI applications. Such highly integrated systems require a multitude of materials to support electrical, mechanical, thermal, and chemical properties. In addition, these materials need to be compatible with packaging processes to ensure compatibility with low-cost manufacturing solutions. The inter-play between the various engineering domains makes the selection of materials, their processability, and compatibility extremely complex. In this article, we investigate the future in terms of the requirements posed by materials for HI and survey the past and present work in this area.

Introduction

The proliferation of artificial intelligence (AI) applications has increased the demand for compute performance and memory capacity. This is coming at a time when the semiconductor industry is facing challenges associated with slowing down of Moore's law. Over the last five decades, Moore's Law has enabled the scaling and integration of compute, memory, and other functionalities on a single silicon chip by increasing transistor density on-chip, while keeping the cost per transistor low. This approach known as system-on-chip (SoC) integrates many functions of the system into a single chip. However, with the slowing down of Moore's Law, the cost of large SoCs has increased exponentially due to two main reasons: (1) the cost/mm^2 of transistors in advanced technology nodes has continued to increase due to increase in technology complexity, and (2) yields have reduced for larger SoCs as we reach the limits of the reticle field. In addition, future electronics is requiring the integration of several IP blocks that may not require the same technology nodes for achieving optimum performance. These limitations and requirements are leaning toward a more cost-effective on-package heterogeneous integration approach to support the growing needs of AI hardware that we refer to here as system-on-package (SoP). Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics.[1]

Two fundamental architectures are currently being pursued by both industry and academia for AI applications referred to as near memory processor (NMP) and processor in memory (PIM). Integration of the CPU, GPU, and high-bandwidth memory (HBM) on a single package, also called an interposer using 2D or 3D connectivity falls under the category of NMP. A better approach is to directly perform computation inside memory, referred to as processor-in-memory (PIM) where the memory array is re-purposed for computation thereby realizing

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massive parallelism and almost nullifying data movement.[2] The fundamental differences between these two approaches relate to three important metrics namely, memory capacity, latency (or delay), and energy consumption. As applications emerge in AI, there is a need for continuous interaction and learning from the environment. This requires neuro-evolution in hardware, where inferences need to be supported in the absence of pre-trained deep neural networks (DNN) and labeled datasets. For such architectures, data movement with low energy per bit (EPB) and high-bandwidth density become critical. As AI architectures become more prevalent, there will be a need for integrating additional chips from domains such as analog, radio frequency (RF), sensing, and photonics along with the compute domains from different process nodes, leading to extreme heterogeneity as shown in **Figure 1**.[3]

The HI architectures can be implemented using a variety of packaging platforms broadly classified into 2D and 3D approaches (Figure 1). In the 2D approach, bare dies (or chiplets) are placed side by side and connected to each other through interconnections in the package substrate. Interposers can be viewed as a large chip consisting of several smaller chiplets connected to each other that also serves the role of a conduit between the dies on top and package substrate at the bottom. In contrast, in the 3D approach, dies are vertically stacked and connected to each other using through-silicon vias (TSVs) and other chip bonding technologies along with non-TSV-based solutions. A variety of materials and package constructions are possible in the 2D and 3D approaches, where these embodiments differ from each other in bandwidth density, energy per bit (EPB), power delivery efficiency (η), and thermal design power (TDP). These represent important metrics that need to be addressed as we progress towards extreme heterogeneity for future AI systems. In the following sections, we investigate the role of materials in supporting these metrics.

Materials for meeting bandwidth density and EPB metrics

Bandwidth density refers to the number of bits transmitted and received between dies per mm (millimeter) for 2D and per mm^2 for 3D. This is largely dictated by the wiring density, wire length, and signaling data rate on each wire. Today, for 2.5D interposers, the bandwidth density is in the range 500–5000 Gbps/mm, while for 3D, the range is 1–5 Tbps/mm^2. With a trend towards big data, there is a continuous need to increase the bandwidth density even further through miniaturization, as shown in **Figure 2**. The wiring density is determined not only by the photosensitive materials (photoresists or photo-imageable) used but also the lithographic process and tooling required for patterning and etching. The ability

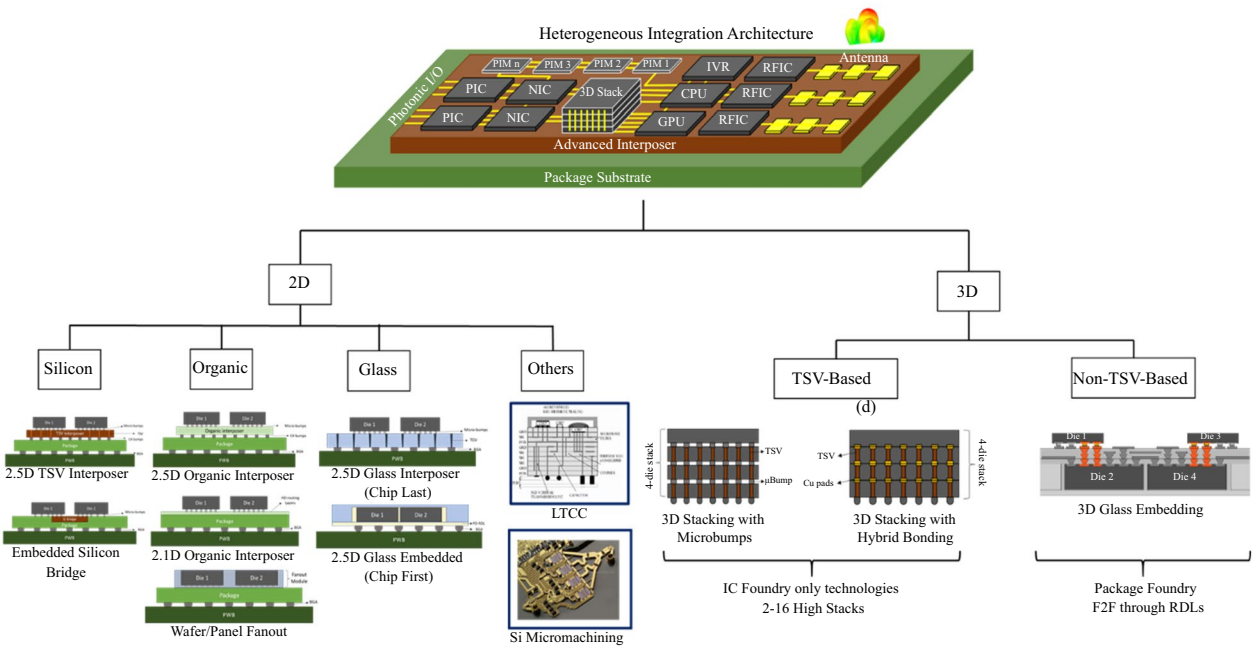
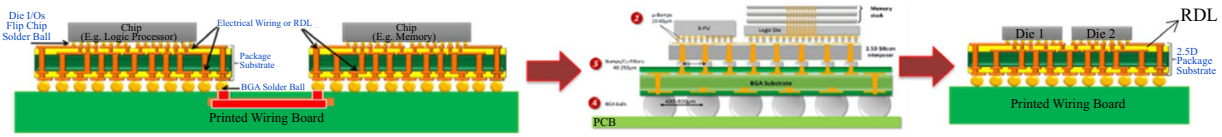


Figure 1. HI Architecture supporting compute, communication, sensing and control functionality (top), and Advanced Packaging Solutions using 2D and 3D approaches (bottom). Two-dimensional solutions represent high-density packaging also called 2.5D. Silicon, organics, glass, and ceramics are the substrate materials of choice for 2D integration. Through-silicon via (TSV) interposer, embedded silicon bridge (EMIB), organic interposer, wafer & panel level fanout, glass interposer (chip last/first), low temperature co-fired ceramic (LTCC), and micromachining are examples of 2D approaches. Similarly, TSV and non-TSV-based stacking using microbumps, and hybrid bonding are examples of 3D integration. With 3D integration, either an integrated circuit (IC) or package foundry can be used for manufacturing based on the construction. RDLs redistribution wiring layers.



System-on-Board | Logic + Memory on Interposer | Heterogeneous Integration

Figure 2. Heterogeneous integration requires high wiring density with fine pitch lines and spaces in the redistribution wiring layers (RDLs).

to communicate between dies with high-bandwidth density at low EPB requires low wire capacitance, which translates to shorter wires between dies and low dielectric constant materials. The integration of ultra-low D_k (ULK) materials in the redistribution wiring layers (RDLs) of the package therefore becomes a major requirement.

There are several material candidates that have low dielectric constant that have been developed for applications using back-end-of-the-line (BEOL) processes.[4–7] **Table I** lists the polymers used by industry that have a dielectric constant (D_k) of 3 or more. This is primarily since ULK materials ($D_k < 2.5$) need to be qualified based on several different properties of polymers. Table I also shows the properties of the polymer dielectrics that are needed in systems for AI and high-performance computing (HPC) applications.

A critical property of ULK materials for packaging applications is their coefficient of thermal expansion (CTE). For the package to be reliable, the ULK dielectric material should exhibit a CTE close to that of the copper metal layer. For ULK materials, this is hard to achieve owing to the inability to use filler particles which increases the dielectric permittivity of the polymer. The filler particles used are typically SiO_2 ($D_k = 3.9$), and since the fillers need to be loaded in high volume/weight% compared to neat polymer dielectrics such as fluorinated polymers, they do not help reduce the D_k value. The presence of added fillers in polymer dielectrics used as build-up layers also becomes a bottleneck for scaling of microvias. To achieve highest wiring density with fine lines and spaces, the diameter of the microvias should be comparable to the line width and spacing. The ULK polymers containing highly fluorinated monomers create additional challenges in the form of reduced adhesion of both polymer on copper and copper on polymer. This is a formidable task since it requires careful selection of adhesion promoters and surface treatments for achieving reliability of the fabricated structures by overcoming delamination during environmental and accelerated aging studies. This is an area of ongoing research at panel scale for packaging. Additional challenges such as plating and seed layer etching arise while scaling to panel level processes since semi-additive processing (SAP) is the preferred method for RDL fabrication.

Aside from low dielectric permittivity materials, there is also a renewed interest in photo-imageable dielectrics (PID) particularly for high-density interconnects. This interest arises from two aspects: (1) number of steps used in the SAP process can be reduced by employing PIDs as the need for photoresists is eliminated, and (2) PIDs can impart better resolution in terms of fine line patterning.[8] However, all the currently available PIDs have a dielectric constant >2.5 which represents a major roadblock for achieving high density, low capacitance, and high aspect ratio fine line interconnects.

The research work being pursued at the Packaging Research Center (PRC)[2,9–17] is directed towards achieving very high wiring density with fine lines/spaces (<1 µm) that include dielectric build-up layers with a dielectric constant <2.5 and polymer microvias with diameter <2 µm. This research is also directed towards using the SAP process that is compatible with panel-scale processes and is essential for fabricating large body size interposers. Furthermore, it is equally important to develop panel-scale processes using ultra-thin dielectrics with high surface planarity to support fine lines and spaces. The surface planarity of the polymer dielectric becomes critical when the line width and space are less than 2 µm as thickness variations over the length of the panel will affect the yield of the fine line features.

Materials for increasing power delivery efficiency

The power delivery efficiency η represents the ratio of the power delivered to the die to the power delivered to the voltage regulator (VR). The efficiencies are typically in the range 75–80% for high-performance computer applications. These efficiencies can be increased by either decreasing the effective resistance between the VR and die or/and integrating high-voltage conversion ratio regulators near the die on the same package.[18] For such integrated voltage regulators (IVR), the inductor serves as an energy storage element by delivering current to the output. The key performance metrics which are used to judge the performance of inductors are its energy density, quality factor, and saturation characteristics. This requires the integration of new magnetic materials capable of high-frequency operation. Another key aspect of power delivery to the chip is managing the voltage drop that comes from the parasitic loop inductance in the power delivery network (PDN) during events of spike in load current of the chip. Decoupling

Table I. (Left) dielectrics currently used in some of the commercially available as well as advanced packaging solutions ULK;[5–15,77] (right) key properties required for ULK dielectrics

	Material	D_k	RDL, line/space	Thickness of Dielectric	Process	Type of package	Key Properties	
Shinko's organic interposer (i-THOP)	Photosensitive-resin	3.0–3.5	2/2 μm (R&D)	>10 μm	SAP	Interposer (panel)	Processability	Thickness Dry film vs liquid; lamination vs spin-coating, other casting methods
Amkor (SWIFT)	Polyimide (PI)	3.0–3.6	2/2 μm (R&D)	>15 μm	SAP	Fanout (wafer)	Adhesion to copper plated substrates	Copper to polymer; copper to substrate Surface roughness; filler size planarization: fly cut, CMP Polymer to copper; polymer to substrate
SEMCO	Polybenzoxazole (PBO)	3.1	2/2 μm (R&D)	>5 μm	RDL first	Fanout (panel)	Surface planarity of films	Surface roughness; filler size planarization: fly cut, CMP
Amkor (SLIM)	Silicon oxide	4	<2/2 μm (R&D)	>2 μm	BEOL	Interposer (wafer)	Mechanical reliability	Warpage of films; residual stress; elongation to break
Intel EMIB	Silicon oxide	4	2.2 μm (product)	>2 μm	BEOL	Fanout (panel)	Coefficient of thermal expansion (CTE)	Low CTE Close to copper (17–18 ppm/°K) or substrates such as glass (3–9 ppm/°K); silicon (3 ppm/°K); organics such as FR-4 (E-glass filled; 16–20 ppm/°K)
Xilinx	Silicon oxide	3	<0.5 μm (product)	>2 μm	BEOL	Interposer (wafer)	Electrical reliability	Moisture absorption Leakage current Electrochemical migration Barrier layer materials
Cisco	–	–	6/6 μm (product)	–	SAP	Interposer (panel)		
Kyocera APX	–	>3.0	6/6 μm (R&D)	–	SAP	Interposer (panel)		
Glass Interposer	Epoxy	3.0	2/2 μm (R&D)	<3 μm	Embedded trench	Interposer(panel)		

capacitors at multiple stages of the PDN keep the impedance spikes below tolerance across broad frequency ranges. However, the size, equivalent series resistance (ESR) and series inductance (ESL), and cost of the decoupling capacitor play a crucial role in determining the quality of power delivery, especially with the number of power rails being more than 50 in modern computing applications.[18]

The trend for power delivery in HI is shown in **Figure 3**, where the objective is to maximize the power density while reducing interconnect length and module thickness. This requires the integration of two critical components namely, inductor and capacitor. Miniaturization of these components along with integration beneath the die shadow requires high-permeability magnetic materials and high D_k materials, respectively, as shown in Figure 3.

Magnetic materials

Magnetic materials are chosen based on, (1) permeability at the desired operating frequency, (2) ferromagnetic resonance frequency (FMR), (3) loss tangent (ratio of real part of permeability (μ') to complex part of permeability (μ'')), and (4) saturation magnetization. Magnetic materials are usually used in the form of powdered cores, metal polymer composites, and thin films that are easily processable. Factors influencing magnetic properties of the material are (1) alloy composition, (2) particle size, (3) particle shape,[19] (4) grain size, (5) grain orientation, and (6) process conditions. Alloys with varying percentages of metal constituents have different properties that can be exploited based on the application. When the grain sizes are large enough such that grain boundaries are at a minimum (e.g., Hitachi Metglas®), such materials have good soft magnetic properties including low coercivity, low loss, and high-permeability, which are of importance for a variety of applications.

Ferrites are a class of materials that are used when the required frequency of operation is around 100s of kHz. Ferrites typically have lower saturation magnetization and low permeability. Although with some modifications, ferrites can be extended to applications in the few 10s of MHz range, they are not preferred when compared to metal alloys which are the materials of choice in the MHz range. Soft magnetic alloys like Fe–Si have higher permeability but use of these materials at higher frequencies leads to significant losses, since the permeability of these materials increases depending on the weight percentage of Si. With addition of silicon, the permeability increases to its highest value at 6.5 wt% of Si (Fe93.5Si6.5) and decreases upon continued addition of more silicon.[20] Other soft magnetic materials include alloys of nickel, zinc, and cobalt which typically have high magnetization saturation and high permeability. However, due to their high conductivity, they generate eddy currents at high frequencies. This has been addressed by use of low conductivity elements like boron, phosphorus, and oxygen which help in reducing the eddy current losses.[21] The presence of oxide/phosphate on metal particles keeps the eddy current losses low by reducing contact between adjacent particles thereby reducing eddy current loop, which, however, reduces the permeability as well. Metal polymer composites exhibit better properties as the metal particles are dispersed in a polymer matrix which prevent longer eddy current paths. The permeability of polymer composites is influenced by the amount of loading and shape of the particles. For example, flake-shaped particles have higher x–y plane permeability when compared to spherical ones. Due to this reason, metal polymer composite sheets with metallic particle flakes are being investigated actively as possible candidates for package-embedded inductors.

Size of the metallic particles in polymer composites plays a significant role as the particle size is proportional to the eddy current losses. Mechanical deformation during

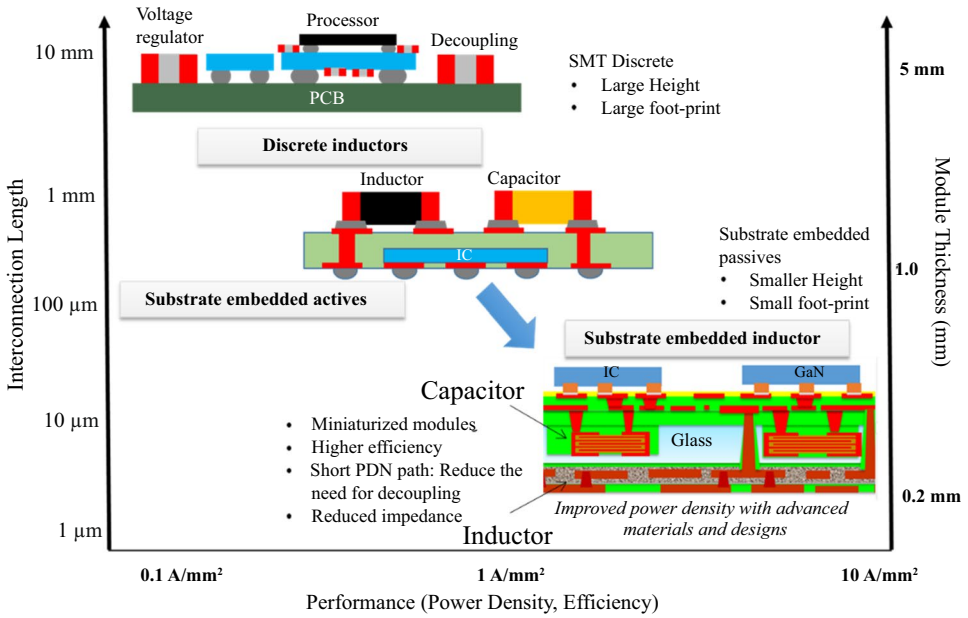


Figure 3. Trend for power delivery using embedded inductors and capacitors using high-permeability magnetic materials and high-permittivity dielectric materials. SMT, surface mount technology; PDN, power delivery network; IC, integrated circuit.

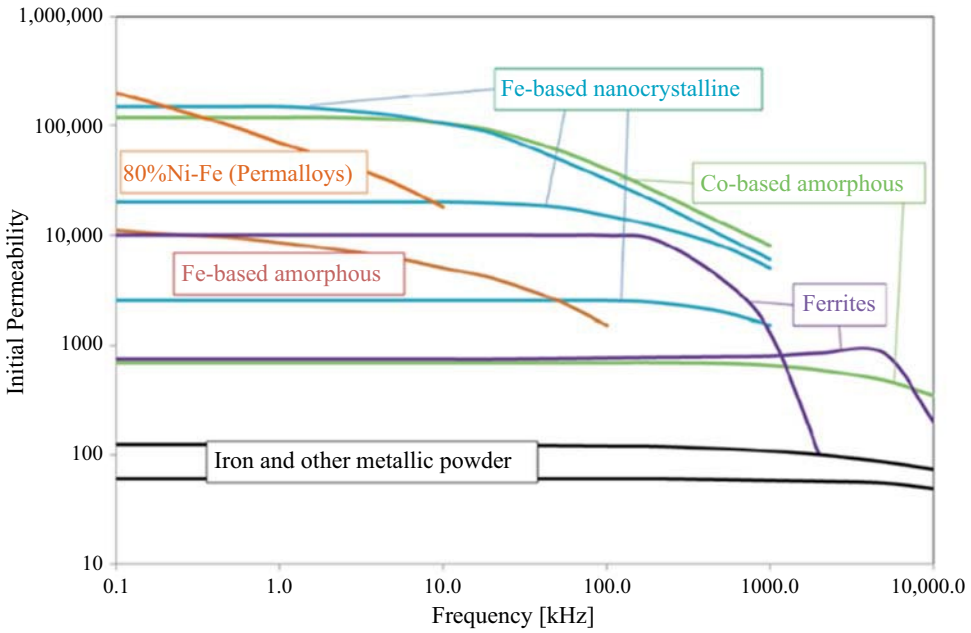


Figure 4. Permeability versus frequency for various classes of materials.[26]

processing has a detrimental effect on the soft magnetic properties as well.[22] Usually, materials used at RF frequencies have been fabricated through low throughput methods such as sputtering.[23–25] Although thin films have high FMR, they are limited by their current handling capabilities which limit their application in power delivery.

Figure 4 shows the operating frequency range for various classes of magnetic materials. In the recent past, materials exhibiting high-frequency stability have been demonstrated. Trade-offs between frequency stability, permeability, and losses must be considered when designing and synthesizing magnetic materials.

The permeability for magnetic materials reported in the literature is in the range 5–1000, with magnetic loss tangent of 0.01–1 and FMR of 1–100 MHz. For composite materials, an important exercise is to optimize the volume fraction of the metal particles thereby increasing FMR frequency while reducing magnetic loss tangent, with a reasonable permeability. As we move towards higher voltage IVRs using stacked FinFETs or GaN-based devices, the target switching frequency is in the 5–50 MHz range. This allows for a relatively small inductor while keeping switching losses manageable. Based on a trade-off between saturation current, inductance density, and DC resistance, the required properties of the magnetic material can be derived using the Lorentz and Landau–Lifshitz–Gilbert equation.[18,27] As an example, for a 48 V/1 V conversion @ 10 MHz with 90% efficiency, the magnetic material should have a permeability of ~90, loss tangent less than 0.033 at 10 MHz and stability up to 50 MHz.[28] However, most commercially available high-permeability materials have a loss tangent that is unacceptably high at frequencies of 10 MHz or higher, which becomes a bottleneck.

Dielectric (high D_k) materials

There is a demand for capacitors with ultra-high volumetric densities in smaller form-factors. Additionally, to minimize the power wastage in granular power management systems, thinner capacitors are needed that determine the overall efficiency.

Industry is making use of embedded discrete capacitors in their processor packages. The low inductance provided by placing capacitors closer to the die is desirable for supporting high-bandwidth processing. Intel demonstrated the impedance benefits of embedding capacitors in the substrate, directly beneath the die, in addition to surface-mount capacitors on the opposite sides of the substrate. A significant drop in impedance was observed from 5 to 300 MHz, especially around the power supply spike at 130 MHz, which exists when decoupling capacitors are placed far from the die.[29]

Multilayered co-fired ceramic capacitors (MLCCs) provide high volumetric capacitance density at low cost and are available for board-level assembly using standard surface-mount technologies (SMTs). More recent advances in materials have led to high-permittivity dielectrics for miniaturization by adding ferroelectric fillers to dielectric laminates to increase the dielectric constant. In the early 2000s, Motorola developed a photo dielectric with a permittivity of 20–22 using this concept.[30] Similarly, 3M has developed embeddable laminate capacitor with copper thickness down to 6 μm that can achieve up to 6.2 nF/cm^2.[29] Although inorganic materials such as $BaTiO_3$ and $SrTiO_3$ provide very high dielectric constants ~2500, owing to the difficulty in processing these materials, package integration becomes difficult. However, by using polymer nanocomposites consisting of barium titanate nanoparticles (30–50 nm diameter) with suitable surface modifiers such as phosphonic acids, D_k between 20 and 50 can be attained with low temperature processing in thin films.[31] Organically modified sol–gel material with D_k ~20 [32] have also been reported which can be processed at temperatures <120°C with a wide range of film thicknesses.

While integrated ferroelectric ceramics are an attractive option for higher capacitance densities, ceramic capacitors require high-temperature processing due to the solid-state diffusion reaction between $BaCO_3$ and TiO_2 particles that takes place at 950–1200°C.[33] These firing temperatures are incompatible with the rest of the package process (exception being LTCC) and, thus, are primarily used as discrete components formed separately. To form ceramic capacitors directly on-chip, lower processing temperatures are required. Much effort has been focused on using sol–gel processing to achieve this, which only requires a final high-temperature annealing step.

Silicon-integrated trench capacitors are much more compatible with on-chip decoupling than ceramic capacitors. Therefore, developmental work has focused on enhancing their capacitance to compete with ceramics. This is largely enabled by advanced etching and deposition processes. For example, Apple's A10 processor used land-side decoupling with silicon deep-trench capacitors from TSMC.[34] The insertable silicon chip capacitors can be embedded into the package, as Apple did in their integrated DRAM-logic module. The capacitors can attain up to 500 nF/mm^2 down to 100 µm thickness. Since the capacitors are based on paraelectric silicon dioxide dielectric, they have superior voltage and temperature coefficients of capacitance and are available up to 4.5 V rating.

Electrolytic capacitors have potential to provide some of the highest volumetric densities owing to their ultra-high surface areas and thin dielectrics. However, they are generally formed as pressed pellets or wound sheets, which make them bulky. A new design that uses a panel scalable, single-etched aluminum sheet has been developed to overcome this challenge.[35] A combination of high surface area from etched Al sheet and conducting polymer cathode layers yields high capacitance density without the high-temperature constraints. These capacitors can then be released on the chip using a foil-transfer process. PRC has demonstrated embeddable tantalum capacitors of ~100 µm thickness[36] with a density >2 µF/mm^2 at 1 kHz and >1 µF/mm^2 at 1 MHz. The tantalum nanoparticle anode is printed on a tantalum carrier foil as a paste before sintering. The carrier foil with capacitor layer is then transferred onto the wafer or package. A cross section of the thin-film capacitor is shown in **Figure 5**.

The increase in capacitance density of silicon capacitors like MIM capacitors have made them good candidates for filtering the output ripple in high-frequency IVRs. Recent improvements in deep-trench capacitor technology could make them a good candidate for providing sufficient decoupling even down to 10 MHz. One problem with currently available silicon capacitors is their inability to handle high voltages. As we move towards high-voltage IVRs with higher input voltage, we will need high-frequency decoupling for the input rail that can handle higher voltage. One possible alternative to high-voltage silicon capacitors is the development of high-voltage, high-frequency package capacitors such as thin-film capacitors[18,37] and embedded array capacitors.[38]

Materials for managing thermal design power

The thermal design power (TDP) represents the sustained maximum power that a computing element can support while keeping the die junction temperature below its maximum allowable limit, which is typically around 100°C. It is calculated as the ratio between the temperature difference (ΔT) and effective thermal resistance, where ΔT is the difference between the die junction and ambient temperatures.

A large contributor towards the effective thermal resistance is the thermal conductivity of thermal interface materials (TIMs). They are used in flip-chip packages and embedded fanout packaging, shown as TIM1 (between die-to-heat spreader) and TIM2 (between heat spreader-to-heatsink) to remove the heat from the top or bottom surface, as shown in **Figure 6**.

In general, TIM is employed for filling the interfaces between thermal components, where microscale point contacts between rough surfaces of the components result in limited contact surface area and reduced thermal channels through the interfaces. Air in the micro-pockets at the interfaces have an adverse impact on interfacial thermal transport due to its poor thermal conductivity (~0.025 W/mK @25°C) which can significantly increase the interfacial thermal resistance. The thermal conduction dramatically degrades while traveling through the interfaces owing to the interfacial thermal resistance, as shown in Figure 6(c), where decreasing bond line thickness (BLT) and increasing thermal conductivity of the filled interface space help mitigate thermal loss via decreased interfacial thermal resistance. The thermal resistance (R_{TIM}) of TIM can be expressed as $R_{TIM} = BLT/k_{TIM} + R_{c1} + R_{c2}$ where k_{TIM} is the thermal conductivity of TIM. Along with the thermal conductivity of TIM materials, it is very important to secure the interfaces through mechanical adhesion and thermal coupling for mitigating thermal scattering at these interfaces. In addition, Young's modulus and CTE of TIMs are also critical parameters that determine the thermomechanical reliability of the package along with the pressure requirements for bonding to ensure compatibility with package processes.

In general, various types of TIMs are available, for example, in the form of grease (silicone-based matrix filled with thermal fillers/boron nitride (hexagonal-BN)[40] or alumina-Al_2O_3),[41,42] phase change materials (PCM, utilizing latent heat during melting, polyolefin and low Mw polyester),[43–45] gels and adhesives (silicon-nitride[46] or silver-filled epoxy).[47,48] The h-BN and exfoliated h-BN nanosheets (BNNS) have been extensively studied as thermal filler in polymer or ceramic composites with high thermal conductivity and electrical resistivity.[49–62] h-BN is a *z*-direction stacking structure that uses van der Waals bonding of covalently bonded 2D hexagonal boron-nitrogen (h-BN) atoms, which is very similar to the structure and thermal properties of graphite. For insulating TIMs, alumina filler is used for <4 W/mK while alumina/h-BN blend or BN filled TIM can reach ~17 W/mK by controlling filler sizes and morphologies.[63] Besides, low loadings

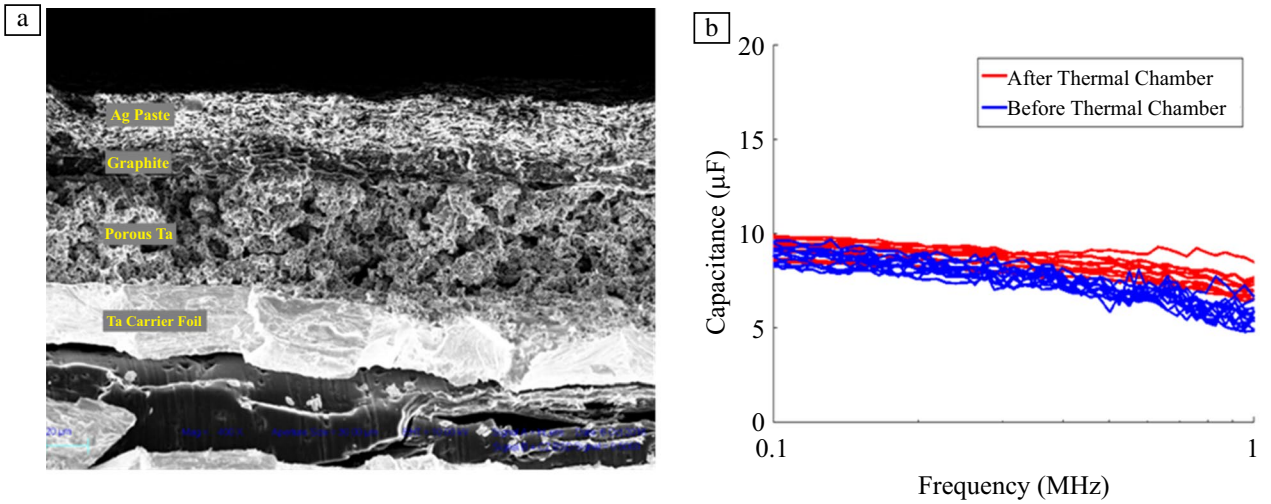


Figure 5. (a) Thin-film tantalum capacitor cross section and (b) capacitance stability with frequency.

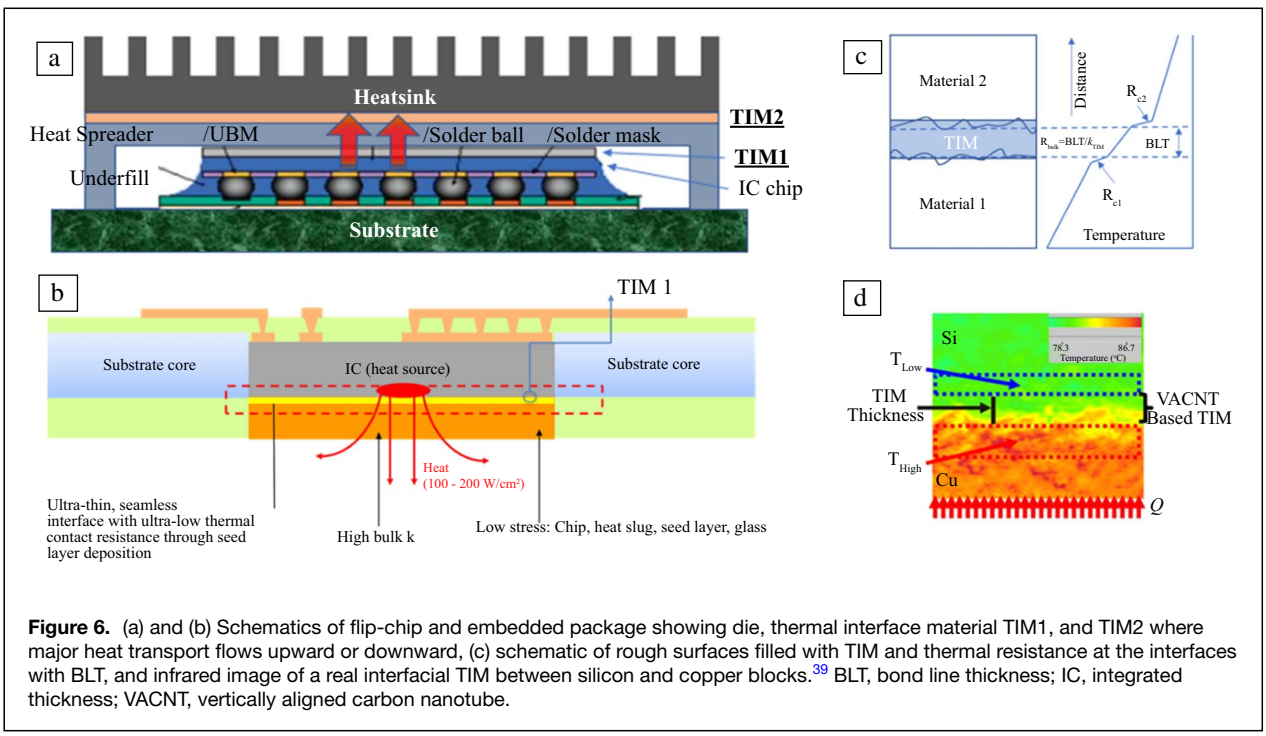


Figure 6. (a) and (b) Schematics of flip-chip and embedded package showing die, thermal interface material TIM1, and TIM2 where major heat transport flows upward or downward, (c) schematic of rough surfaces filled with TIM and thermal resistance at the interfaces with BLT, and infrared image of a real interfacial TIM between silicon and copper blocks.[39] BLT, bond line thickness; IC, integrated thickness; VACNT, vertically aligned carbon nanotube.

of aligned BNNS-filled silicone have exhibited 10–12 W/mK, but the higher loading without compromising viscosity can be challenging to achieve.

Carbon allotropes such as multi-walled/single-walled vertically aligned carbon nanotubes (CNTs),[64,65] aligned graphene nanosheets,[66] graphite nanoplates,[67] carbon black,[68] CNT/metal composite, etc. have recently received much attention for TIM applications due to their exotic thermal conduction performance via ballistic transport (>3000 W/mK). In addition to polymeric and metal/carbon composites, metallic TIMs such as solder alloys have been employed in microprocessor cooling because of their high thermal conductivity. In addition, more solutions such as "wet" solder (liquid metal) TIM by using liquid metal such as Ga that is less toxic with a lower vapor pressure than mercury, such as GaIn, GaInSn, and others have been investigated.[69,70]

Among several approaches to TIMs, high thermal conductivity thermal filler loaded adhesive types of TIMs such as silver (429 W/mK),[36] copper (401 W/mK),[71,72] aluminum (~205 W/mK),[73] transient liquid-phase sintering (TLPS),[74,75] and others in thermoset type resins are promising candidates.

Recent developments on TIM have been focusing on the filler/interface engineering to address the limited thermal conductivity of TIM and its interfacial thermal resistance to bonding substrates, including exploitation of nanosilver sintering at low temperatures in the form of dry metal sintering (>70 W/mK) or fusion in polymer (>30 W/mK) (interfacial atomic/grain boundary diffusion induces metallurgical interconnections between nanoparticles to form the thermal paths).[76]

Summary and path forward

AI applications are driven by the ability to communicate between logic and memory with minimum delay. With the trend towards heterogeneous integration, off-chip communications between dies become important where the delay is dictated by the relative permittivity of the dielectric material used. Lowering dielectric constant not only reduces delay but also the EPB. As the future unfolds, dielectric materials with permittivity less than 2.5 are required which are processable as part of a package stack-up that supports fine line width, small spacing, and microvia geometries for supporting large bandwidth density. Hence, the mechanical, chemical, and thermal properties of the material become equally important. The large number of memory-compute operations often causes a power delivery problem, where large currents must be supplied to the dies causing excessive DC drops and AC noise. This can be mitigated using IVRs operating near the die on the same package. Such implementations require high-density inductors and capacitors embedded in the package, requiring high-permeability magnetic materials and high-permittivity insulating materials. Most magnetic materials are limited by their loss, FMR, and saturation magnetization in the frequency range 1–100 MHz. With high-permittivity materials, a major bottleneck is their ability to withstand high voltages. With most data center implementations having an efficiency in the 75–80% range, any improvements in both magnetic and dielectric materials can have a large impact on energy efficiency. Finally, TIM represents a critical material that is in the heat dissipation path for all dies, and often times becomes the showstopper in our ability to dissipate large heat flux. An ideal TIM would have (1) thermal conductivity better than that of copper that can be directly deposited on the die, and (2) CTE matched with that of the die to ensure reliability.

In this article, we have only focused on four important material systems that are essential for enabling the next generation of AI systems, understanding fully well that there are more materials and interfaces that one needs to address to build highly integrated heterogeneous systems.

Conflict of interest

The authors declare that they have no conflict of interest.

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