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Epitaxial growth and layer-transfer techniques for heterogeneous integration of materials for electronic and photonic devices

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The demand for improved electronic and optoelectronic devices has fuelled the development of epitaxial growth techniques for single-crystalline semiconductors. However, lattice and thermal expansion coefficient mismatch problems limit the options for growth and integration of high-efficiency electronic and photonic devices on dissimilar materials. Accordingly, advanced epitaxial growth and layer lift-off techniques have been developed to address issues relating to lattice mismatch. Here, we review epitaxial growth and layer-transfer techniques for monolithic integration of dissimilar single-crystalline materials for application in advanced electronic and photonic devices. We also examine emerging epitaxial growth techniques that involve two-dimensional materials as an epitaxial release layer and explore future integrated computing systems that could harness both advanced epitaxial growth and lift-off approaches.

Epitaxy — the art of growing single-crystalline films on a crystallographically oriented wafer — has been a key technology for developing modern solid-state electronic and photonic devices on various inorganic substrates. The process can be homogeneous (growth on a substrate of the same material) or heterogeneous (growth on a substrate of a dissimilar material). Homoepitaxial growth typically results in a high-quality single-crystalline epitaxial layer copying the crystal structure of the substrate. Heteroepitaxial growth, by contrast, is generally limited by the requirement for lattice matching between the epilayer and substrate material. For example, monolithic integration of III–V and III–N compound semiconductors on silicon has been of great interest in electronic and photonic communities to compensate for the poor carrier mobility and light-emitting efficiency of silicon-based integrated circuits. However, such approaches have been restricted by the generation of a high density of defects in the epitaxial heterostructure on silicon due to the large lattice and thermal expansion coefficient mismatch between the two materials.

To reduce epitaxial defects and threading dislocations, various epitaxial growth methods have been developed for heteroepitaxy of highly lattice-mismatched materials: low-temperature buffer layer, lattice-engineered buffer layer, metamorphic buffer layer, domain-matched epitaxy and epitaxial lateral overgrowth. These epitaxial growth approaches enable a wide variety of compound semiconductors to be grown on lattice-mismatched substrates by controlling the density of extended defects such as threading dislocations and stacking faults.

Despite such advances, it is still challenging to achieve good crystal quality of heteroepitaxial layers with large lattice mismatch, compared with what can be achieved with homoepitaxial layers, but homoepitaxy often requires extremely expensive substrates. This limits wide adoption of such electronic/photonic materials in major commercial markets. While advanced heteroepitaxy techniques can accommodate relatively large lattice mismatch between the device (active) layer and substrate (often mismatch greater than 10%), direct heteroepitaxy without any form of strain/domain engineering typically forms extremely defective or polycrystalline device layers if the mismatch is more than a few per cent. Thus, monolithic integration of high-efficiency devices via heteroepitaxy becomes complex, expensive and time consuming.

An elegant solution is to lift off and transfer the grown epitaxial layer from the substrate, which allows heterointegration of highly mismatched material systems. The lift-off approach gives the freedom to transfer the released epilayer onto any arbitrary substrate of interest, and also allows the expensive substrates to be reused if the substrate is undamaged during the lift-off process, reducing the overall cost of device production. Various lift-off technologies have been developed, including epitaxial lift-off (ELO), mechanical spalling, laser lift-off and two-dimensional (2D) material-assisted layer transfer (2DLT), in accordance with the growing need for heterogeneous integration of dissimilar materials. In particular, 2DLT requires unique epitaxial techniques such as remote epitaxy or van der Waals (vdW) epitaxy, allowing growth of single-crystalline thin films on 2D materials, which can be easily exfoliated from the weak vdW interface.

In this Review, we first introduce conventional epitaxial growth mechanisms and methods to form epitaxial heterostructures. We then provide an overview of advanced heteroepitaxy techniques for monolithic integration of high-quality device layers to lattice-mismatched substrates with reduced defect densities, and ELO techniques for heterogeneous integration of highly lattice-mismatched systems. These two techniques provide a strong foundation for 3D heterogeneous integration of dissimilar materials, which could provide enhanced functionality and efficiency of electronic and photonic elements on a single wafer (Fig. 1). We also discuss emerging epitaxial growth techniques that involve 2D materials as an epitaxial release layer. Finally,

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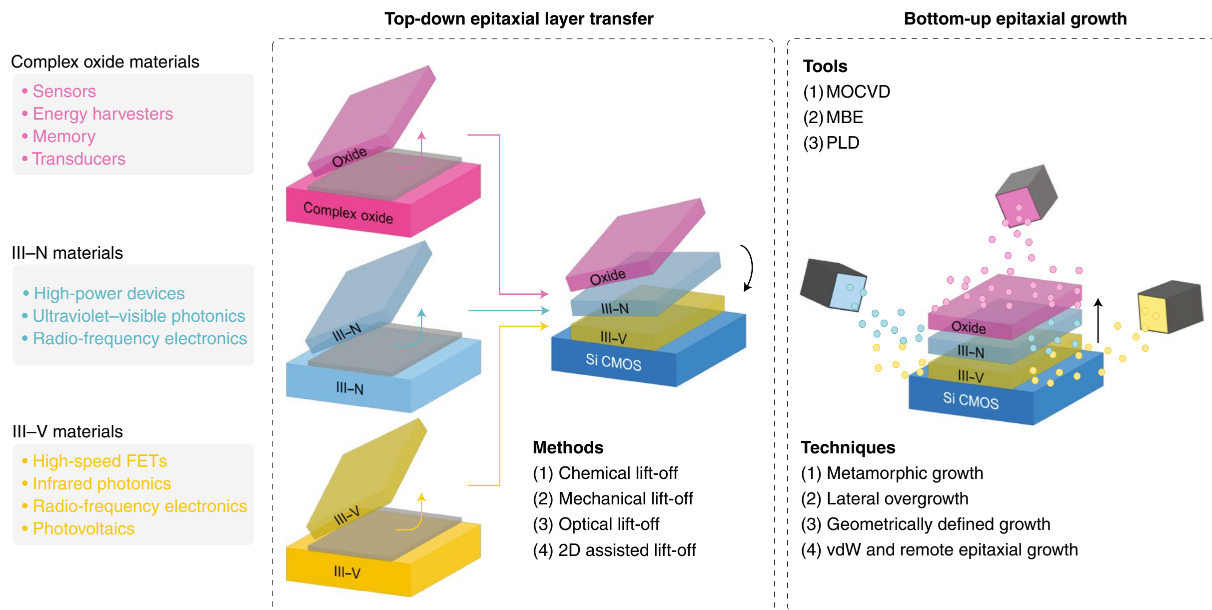


Fig. 1 | Overview of heterogeneous integration of dissimilar materials for electronic and photonic applications. Schematic of top-down (epitaxial lift-off and transfer) and bottom-up (epitaxial growth) methods of heterogeneous integration of various crystalline materials relevant to the electronic and photonics industry. Both epitaxial layer-transfer and epitaxial growth techniques allow integration and coupling of dissimilar materials for enhanced and improved functionality of conventional semiconducting platforms. The most relevant materials in the electronics and photonics industry (apart from silicon) include III–V materials, which are low bandgap with high mobilities, III–N materials with high bandgap and optimal for high-power electronics, and insulating complex oxide materials with multiple physical properties (superconductivity and robust ferroic properties) promising to enhance conventional silicon systems with added functionalities. MOCVD, metal–organic chemical vapour deposition.

we explore future integrated computing systems that could harness both advanced epitaxial growth and lift-off approaches.

Conventional epitaxial growth techniques

Epitaxial growth (Box 1) of homogenous materials (Fig. 2a) is relatively straightforward. However, heteroepitaxy, the growth of an epitaxial film on a substrate of a different substance, is typically not a straightforward process. Yet, heteroepitaxy not only offers the capability to integrate device layers on cost-effective substrates but also provides a path towards realizing efficient and functional devices by combining multiple layers of thin films with different electronic, photonic, magnetic and phononic properties, and thus great efforts have been made to grow heteroepitaxial layers with high material quality. The major challenge in heteroepitaxy comes from strain in epitaxial films[1]. The heteroepitaxial layer has different material properties to the substrate by definition, and among the properties, the mismatch in the lattice constant and thermal expansion coefficient are major sources of strain, along with defect-related strain[2]. Elastically strained pseudomorphic heterostructures (Fig. 2b) can sustain up to a certain thickness, known as the critical thickness (h_c), which is determined by the interface area and the amount of lattice mismatch[3,4]. The h_c of a thin film is on the order of a few nanometres when the lattice mismatch is above a few per cent[5], meaning that lattice matching is a stringent requirement to achieve dislocation-free epitaxy. Above h_c, it is energetically favourable for the strain to relax by forming dislocations. These dislocations can severely deteriorate electrical and optical properties of epilayers by acting as non-radiative recombination centres, and thus engineering the dislocations in heteroepitaxy is critically important in most device applications. A general description of the interplay between misfit strain, thermal strain and defect-related strain during heteroepitaxy across the misfit spectrum is given in ref. [2]. However, large lattice mismatch between two materials does not necessarily lead to deteriorated material quality. A well-known growth paradigm, domain matching epitaxy (DME), allows high-quality epitaxial growth of materials with large lattice mismatch by matching the domains where integral multiples of the major lattice planes are matched across the interface[6]. This paradigm has been invoked to grow high-quality TiN on Si(100), AlN on Si(111) and ZnO on αAl_2O_3(0001), all of which have a large lattice mismatch between 15% and 25%, demonstrating the possibility of monolithically integrating III–V and III–N materials, oxides and silicon on a single wafer via epitaxial growth. Moreover, judicious implementation of DME results in h_c being approximately one to two monolayers, confining the majority of defects at the interface, which results in relaxation of strain without the need of any dislocation nucleation barrier. An in-depth discussion and overview of DME is presented in a seminal article by Narayan et al.[6].

Introducing buffer layers in between the device layer and the substrate is a widely used technique to acquire high-quality device layers, by confining dislocations within the buffer. Low-temperature-grown buffer, for example, suppresses island-like Volmer–Weber growth while promoting relaxation and layer-by-layer growth at an early stage of growth, which is beneficial to the subsequent growth of a high-quality target epitaxial layer at elevated temperatures. As an example, a low-temperature AlN buffer layer was used before the growth of GaN on sapphire substrates, which has approximately 16% lattice mismatch with GaN (ref. [7]). Such a technique directly resulted in the consecutive successes in GaN-based device development as device-quality GaN was obtained for the first time on sapphire substrates. Another type of buffer is lattice-engineered buffers such as superlattices and graded composition layers. Superlattices are composed of multiple thin layers of altering lattice constants, which act as a dislocation filter by bending the propagating direction of threading dislocations. It has been shown that the threading dislocation density can be reduced by more than three orders of magnitude by embedding multiple layers of superlattices under device layers, and this approach has enabled continuous-wave

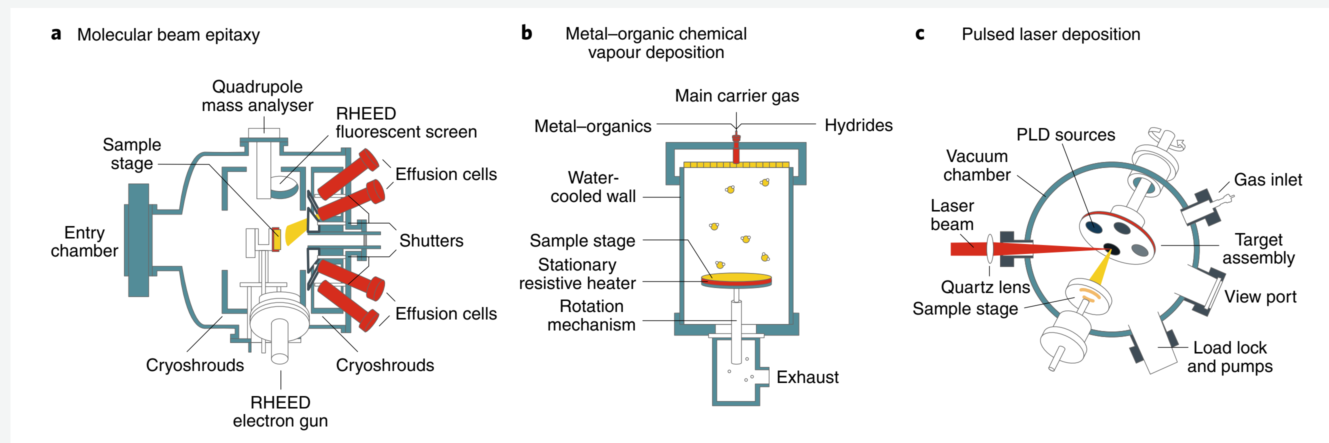
Box 1 | Epitaxial growth tools

Here we introduce three commonly used growth techniques: molecular beam epitaxy (MBE), metal–organic chemical vapour deposition (MOCVD) and pulsed laser deposition (PLD). These three tools mainly differ in the type of sources used, growth conditions and growth dynamics, where all three methods produce high-quality single-crystalline films[115,116].

MBE uses ultrahigh-vacuum ($<10^{-10}$ torr) evaporation techniques for the growth of epitaxial layers on a heated crystalline substrate by molecular beams from constituent ultrapure source materials[117]. It is possible to precisely control the layer thickness in monolayer resolution, material purity, doping concentration and alloy composition. The general MBE system (panel **a**) consists of effusion cells with constituent elements pointing and arranged around the substrate to ensure epitaxial surface uniformity. The epitaxial growth process occurs when a flux of molecular beams generated from the heated sources impinge on the heated crystalline substrate, giving rise to chemical reaction of constituent elements on the surface of the wafer. Growth in MBE largely depends on a kinetic process such as adsorption, desorption, incorporation, migration and reaction. The MBE system is a powerful epitaxial growth tool for studying fundamental science and production of extremely high-quality single-crystalline compound semiconductors for high-performance electronic/optoelectronic devices.

MOCVD is the preferred epitaxial equipment for large-volume manufacturing owing to its relatively fast growth rate (>2–5 μm h^{-1}) and excellent uniformity across large wafer sizes[118]. Due to these advantages, the use of MOCVD for compound semiconductor growth has dominated the market in the past decade. MOCVD (panel **b**) utilizes metal–organic compounds and hydrides as precursors, which are supplied to the reactor by carrier gases such as H_2 and N_2. The precursors then decompose into the growth materials and adducts by pyrolysis at the growth temperature. MOCVD growth is typically performed in low vacuum (50–100 torr), while growth at higher vacuum or atmospheric pressure is also possible.

PLD (panel **c**) has also emerged in recent decades as a means of growing epitaxial films of oxide materials. PLD requires a low-pressure system in the presence of precursor gases such as O_2, N_2 and H_2, where pulses of lasers are 'shot' to ablate a target with the desired source material and deposit the ablated material onto the substrate. During the ablation process, hot dense plasma is formed and reacts with the background gases to form oxides, nitrides or hydrides that deposit onto the substrate to create stoichiometric films. The deposition rate can be precisely controlled by the rate of laser shots and the number of shots, with a growth rate comparable to MOCVD at ~2–5 μm h^{-1} (ref. [119]) as well as accommodate large-area wafers for production. Thus, PLD offers an attractive means of creating artificially layered oxides for fabrication of oxide electronic and magnetic materials and is a versatile tool for fabricating films of ferroelectric, piezoelectric, pyroelectric and magnetic materials[120].



RHEED, reflection high-energy electron diffraction. Figure adapted from: **a**, ref. [121], Elsevier; **b**, ref. [122], AIP Publishing; **c**, ref. [123], Springer.

and room-temperature operation III–V lasers on silicon platforms[8]. In graded metamorphic buffers (Fig. 2c), however, the composition of the buffer layer is gradually changed either linearly or as a step function to slowly alter the lattice mismatch, from which the nucleation of new dislocations is minimized while the glide velocity of dislocations to the interface is maximized[9,10]. Graded composition buffer layers have been proven to achieve significantly improved material quality at the device layer for III–V, III–N and SiGe material systems, by localizing the dislocation at the metamorphic buffer layer. For example, a metamorphic $Si_{(1-x)}Ge_x$ buffer layer with linear grading of Ge composition from 0% to 30% enhanced the electron mobility by twofold, compared with an abrupt $Si_{0.7}Ge_{0.3}$/Si heterostructure[11]. A metamorphic buffer layer has also been utilized to achieve a record-breaking triple-junction solar cell with an efficiency of more than 41%[12].

Epitaxial lateral overgrowth (ELOG) is another lattice engineering technique to realize drastic dislocation reduction (Fig. 2d). In this case, the substrate surface is covered by a patterned mask (usually a dielectric film such as SiO_2 or SiN_x), which has a negligible sticking coefficient to the target material, revealing only small parts of the substrate. The target material grows on the exposed substrate areas and subsequently expands laterally on top of the mask to create a planar film. The ELOG region is dislocation free, hence drastically reducing the dislocation density in the epitaxial film. Using this technique, monolithic integration of single-crystalline III–V on a silicon substrate has been demonstrated, such as GaAs- and InP-based lasers[13,14], which shows its potential to be compatible with current complementary metal–oxide–semiconductor (CMOS) processing.

Emerging epitaxial growth approaches

Although the conventional epitaxy methods presented above could greatly reduce the dislocation density, the material quality of heteroepitaxial layers is still inferior to homoepitaxial counterparts,

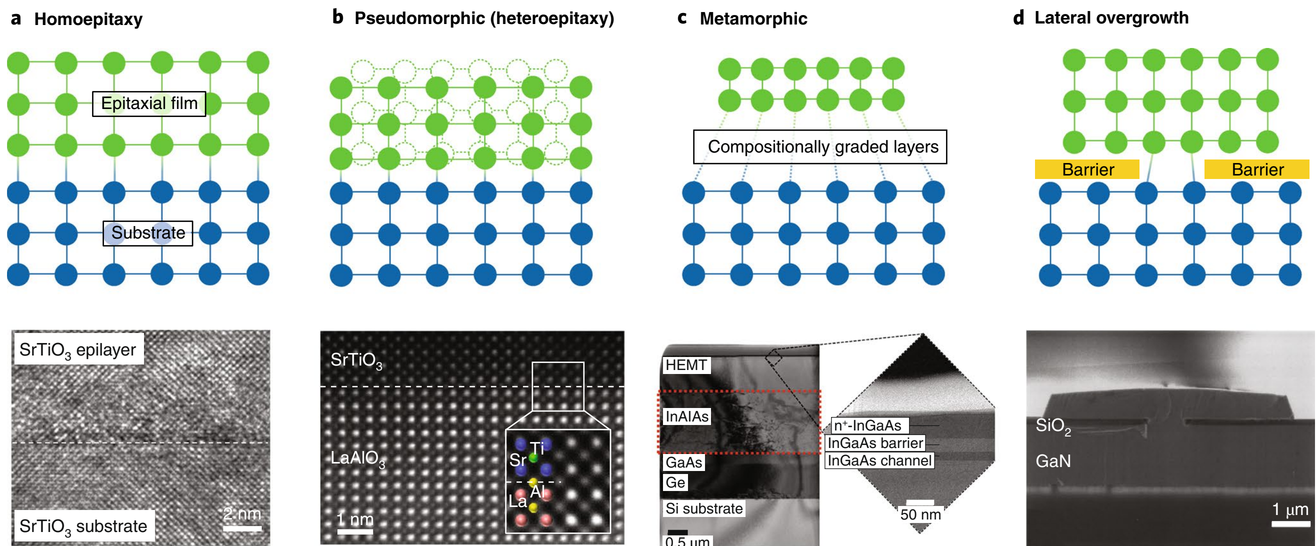


Fig. 2 | Conventional epitaxy techniques. **a**, Illustration of homoepitaxial growth, where the lattice constant of the epitaxial film is matched to the lattice constant of the substrate. The scanning electron microscopy (SEM) image below shows $SrTiO_3$ on $SrTiO_3$ homoepitaxy, where the interface between the substrate and epilayer is difficult to distinguish due to the lattice constant being the same. **b**, Illustration of pseudomorphic epitaxial growth. The epilayer has a different lattice constant than the substrate. The epilayer has to conform to the lattice of the substrate to grow without defects. The original lattice of the epilayer is shown with dotted lines and the strained epilayer is shown with solid lines. If the epilayer thickness increases beyond the 'critical thickness', it becomes energetically favourable for the strain to relax by forming dislocations. The SEM image below shows $SrTiO_3$ on $LaAlO_3$ that is pseudomorphically grown. The lattice constant of $SrTiO_3$ is 3.905 Å, whereas the $LaAlO_3$ lattice constant is 3.787 Å, which has 3.1% of lattice mismatch. **c**, Illustration of metamorphic growth technique, in which a thick buffer consisting of compositionally graded heterostructure is used to gradually change the lattice to match the active epilayer. In the SEM image below, an InAlAs metamorphic buffer is used to grow low-defect InGaAs high-electron-mobility transistor (HEMT) on a silicon substrate. **d**, Schematic of lateral overgrowth (or selective area epitaxy), where an inert oxide mask is used to define small areas where heteroepitaxy occurs. The epilayer grows laterally outside the mask and merges into a complete film, leaving the defects localized in the area of the holes. The SEM image below shows lateral overgrowth of GaN on a sapphire substrate with a GaN buffer using SiO_2 as the mask. Figure reproduced from: **b**, ref. [109], Springer Nature Ltd; **c**, ref. [110], AIP Publishing; **d**, ref. [111], AIP Publishing.

especially in highly lattice-mismatched systems. In addition, the use of thick buffer layers is undesirable as it consumes growth sources and decreases production throughput, which is a drawback for industry focused on mass production. Moreover, due to the mismatch of the thermal expansion coefficient, thick buffer layers induce additional strain when the device is cooled down to room temperature from the growth temperature, which can result in wafer bending, cracking and delamination[2]. Thus, innovative approaches are required not only to overcome these strict lattice matching rules of epitaxy but also to enhance manufacturability and adoption. In this section, we give an overview of several emerging epitaxy techniques, dissimilar from conventional techniques discussed in the previous section, to produce large-area single-crystalline epitaxial films. We categorized them into 2D material-assisted epitaxy (Fig. 3a) and geometrically defined epitaxy techniques (Fig. 3b)[15–17]. The former utilizes slippery surfaces of 2D material substrates that can help relax the films before dislocations are introduced into the crystals, and the latter enables geometrical filtering of dislocations in its 3D architectures.

Van der Waals epitaxy (vdWE) is a 2D material-assisted epitaxy technique that has recently attracted attention owing to the possibility of growing heteroepitaxial films with lattice mismatch greater than 60% (Fig. 3a). First discovered by Koma et al.[15,18], vdWE is a method of performing epitaxy of 2D and 3D materials on top of 2D materials or on top of 3D materials with passivated dangling bonds on the surface. Bulk 2D materials exhibit zero dangling bonds at the surface and are held together by a very weak vdW force. Thus, epitaxial strain can be immediately relaxed on slippery 2D surfaces, allowing growth of largely lattice-mismatched materials on top. Because most 2D materials have a hexagonal lattice, bulk materials with similar lattice structure such as III–N materials have shown robust and high-quality growth. For example, the growth of single-crystalline InGaN/GaN blue light-emitting diodes (LEDs) on single-crystal hexagonal boron nitride (hBN) layers has been successfully demonstrated even with substantially high lattice mismatch between GaN and hBN (>25%) by adding a thin AlN layer as a buffer between the hBN and GaN. In addition, the same technique allowed AlGaN/GaN heterostructures grown on hBN to exhibit an electron mobility of 1,100 $cm^2 V^{-1} s^{-1}$ (ref. [19]), which verifies device-quality GaN on hBN. Moreover, due to the weak vdW interaction of the hBN film, the III–N films could be easily released from the substrate using an indium sheet, which opens up further opportunities for heterointegration. Even with >25% lattice mismatch between GaN and hBN, the dislocation density in grown-GaN was estimated to be 8.6×10^9 cm^{-2}.

Remote epitaxy has been recently discovered, where epitaxy occurs through ultrathin graphene layers between the epilayer and the substrate due to graphene being transparent to the Coulombic interaction between the adatoms and the substrate surface (Fig. 3a)[17,20]. In this method, one to two layers of graphene are transferred or directly grown on the surface of the substrate, followed by epitaxial growth of single-crystalline film seeded by the underlying host substrate through graphene. Remote epitaxy of single-crystalline compound materials such as III–V, III–N and I–VII materials has been successfully demonstrated, whereas remote epitaxy cannot be applied for elemental semiconductors such as silicon or germanium owing to the lack of surface polarity of these materials. Compared with vdWE, remote epitaxy can occur in lattice-matched systems, preventing dislocation formation in the epitaxial films. As in vdWE, remote epitaxial films can also be easily released from the

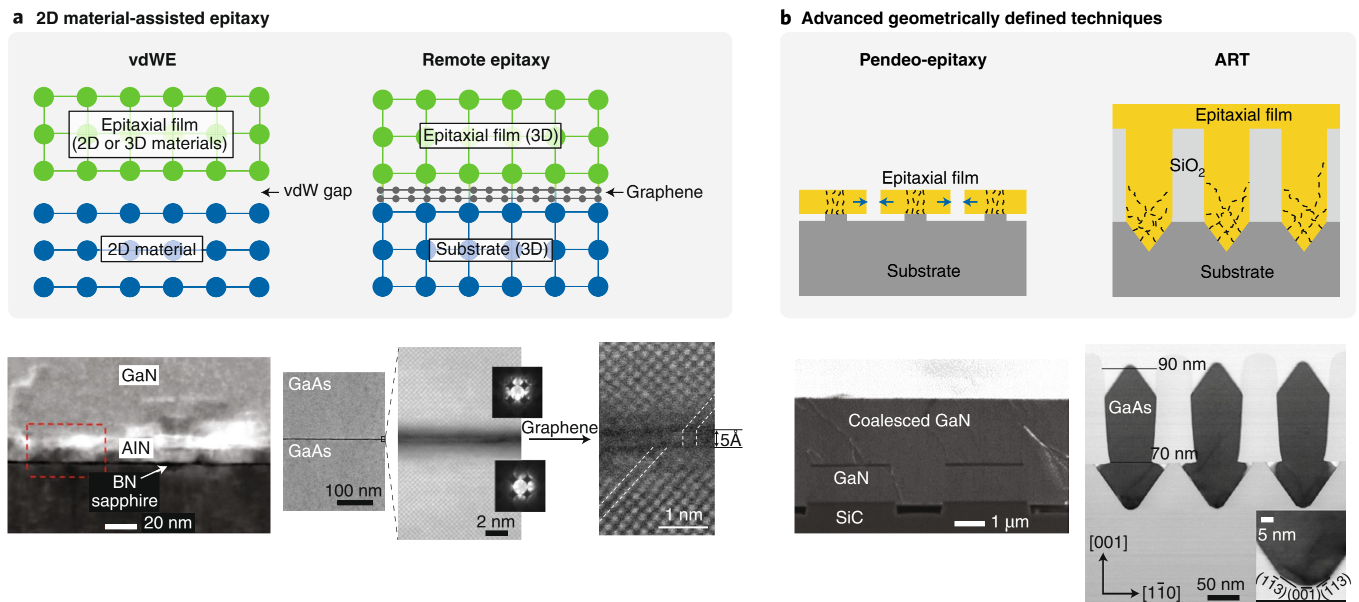


Fig. 3 | Advanced epitaxy techniques. a, Illustration of epitaxy on 2D materials. For vdWE, the epitaxial layer grows without any interaction with the host substrate (schematic, top left). The vdW layer becomes the seed for growth, which can be used to grow single-crystalline materials such as GaN as shown in the cross-sectional SEM image on the bottom left. In contrast, for remote epitaxy, a couple of monolayers of graphene are transferred or directly grown on the substrate and the epilayer is grown directly on top (schematic, top right). The polarity of the substrate penetrates the graphene and the adatoms interact with the substrate as though graphene is not present. However, once the growth is finished, the epilayer can be exfoliated and transferred to any arbitrary substrate since the graphene acts as a sacrificial layer for exfoliation. An example of remote epitaxy of GaAs on GaAs is shown on the bottom right, showing cross-sectional SEM and TEM images of the GaAs/graphene/GaAs interface. **b**, Schematic of geometrically defined epitaxy (top left). Pendeo-epitaxy is similar to lateral overgrowth, but does not use a mask. Instead, small seed pillars are initially grown on the substrate, and the growth condition is modified such that the growth only occurs laterally. A cross-sectional SEM image of pendeo-epitaxy of GaN on SiC is shown on the bottom left. ART uses an inert SiO_2 mask similar to lateral overgrowth, but with much deeper trench (schematic, top right). Due to the deep trench depth, the extended defects are confined in the trench and the resulting film outside the trench is mostly defect free. A cross-sectional TEM of ART of GaAs on Si is shown on the bottom right. Figure reproduced from: **a**, ref. [112] Cambridge Univ. Press (bottom left); ref. [17] Springer Nature Ltd (bottom right); **b**, ref. [113] AIP Publishing (bottom left); ref. [23], AIP Publishing (bottom right).

graphene-coated substrate, which can then be heterointegrated with other materials via layer transfer. Moreover, due to the modified surface energy of the substrate surface by adding graphene, it is possible that remote epitaxy may promote spontaneous relaxation of heteroepitaxial films without generating defects. However, such effects have not been studied in detail and this is an open opportunity for investigation.

Compared with 2D material-assisted epitaxy, geometrically defined epitaxy aims to reduce dislocation density by filtering dislocations inside 3D-fabricated microstructures. One popular geometrical method is pendeo-epitaxy (Fig. 3b). This method is conceptually similar to ELOG; however, there are several key factors that differentiate it from ELOG. First, the substrate is patterned such that a seed 'post' can be grown on selective areas of the substrate. Owing to the lattice mismatch between the 'post' material and the substrate, dislocations are formed in the posts. Once the growth of the 'post' is complete, the growth condition is changed such that lateral growth happens almost exclusively on the sidewalls of the 'post' (there are some variations, but this is the most general description of pendeo-epitaxy). The material continues to grow laterally from the sidewalls until it meets with material grown from an adjacent 'post', converging into a full film similar to ELOG. This method is most frequently used to grow low-defect GaN films. For example, Davis et al. showed pendeo-epitaxy of GaN with low dislocation density on SiC deposited on Si, with GaN seed posts grown on patterned thin AlN buffer layers[21]. A drastic reduction of threading dislocations was achieved, from a dislocation density of 10^9–10^{10} cm^{-2} down to approximately 10^4–10^5 cm^{-2}, as well as a tenfold reduction in leakage currents of a Schottky contact with an ideality factor of near unity.

Aspect ratio trapping (ART) growth is another representative process to geometrically confine dislocations, studied vigorously for III–V films on silicon (Fig. 3b)[22,23]. So far, ART of various single-crystalline III–V materials, such as GaAs, InAs and GaSb, on silicon have been demonstrated, paving the way for monolithic integration of III–V channels with higher mobility on silicon substrates. In this method, V-shaped trenches are etched into the substrate while a large-aspect-ratio mask (typically SiO_2) is fabricated on top to trap and confine the epitaxial layer into the trench. The idea is to confine any extended defects at the bottom of the trench or terminate the threading dislocations at the sidewalls of the SiO_2 mask, allowing a defect-free film to be grown at the upper region of the epilayer where it coalesces into a film. In addition to the reduced density of threading dislocations, this approach significantly suppresses the formation of antiphase boundaries since the nucleation starts from (111) planes. However, this method is reported to still produce twin planes at a density of 10^8 cm^{-2}, which cannot be confined within the trench, and remains a challenge to be solved[23]. Besides the V-shaped trenches, template-assist selective epitaxy (TASE) has been recently demonstrated by IBM, from which the shape of epitaxial III–V materials on Si can be tailored by oxide templates while harnessing the advantages of ART[24,25].

One major drawback of geometrically defined epitaxial methods is that it involves the time-consuming and expensive pre-epitaxy process of patterning the substrate, which involves mask deposition, photolithography, etch processes and extra cleaning steps. So

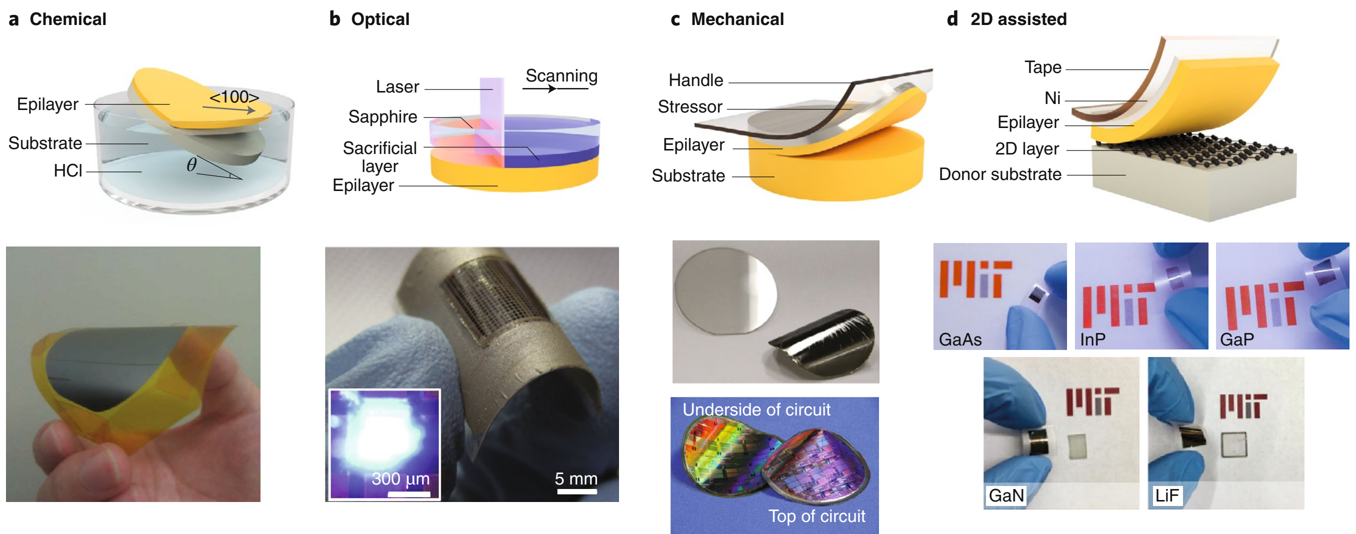


Fig. 4 | Epitaxial lift-off techniques. a–d, Schematics of epitaxial lift-off techniques using a chemically etched sacrificial layer (**a**), an optically induced separation between the epilayer and substrate (**b**), brute-force mechanical spalling using a metal stressor layer (**c**) and 2D material-assisted layer transfer (**d**). The resulting single-crystalline epitaxial membrane is shown below each illustration. Each method has its own advantages and disadvantages, with key parameters being the release-rate, universality of the technique, need for post-release refurbishment of the substrate and controllability of the exfoliated film thickness. In **a**, θ is the immersion angle, and is the angle between the substrate and the HCl solution. Figure reproduced from: **a**, ref. [30], under a Creative Commons licence CC BY 4.0; **b**, ref. [114], Elsevier; **c**, ref. [28], IOP Publishing; **d**, ref. [17], Springer Nature Ltd.

far, the benefits of better material quality using these methods do not justify the extra time and cost required to implement them at an industrial scale. However, we speculate that as heterointegration of vastly dissimilar materials on Si is becoming increasingly important, these methods will be revisited and improved for faster throughput and cheaper cost.

Heterointegration via epitaxial lift-off and layer transfer

Epitaxial lift-off techniques are becoming increasingly important for the fabrication of thin, flexible, lightweight and 3D-integrated structures. The major benefits of epitaxial lift-off techniques are twofold: it allows heterogeneous integration of dissimilar materials, which cannot be otherwise integrated together for expanded functionality; and it allows the host substrate to be reused, which dramatically reduces the fabrication cost of devices[17,26–28].

Several lift-off technologies have been developed so far at the industrial scale. Chemical lift-off is a method of creating freestanding epitaxial films by inserting a sacrificial layer that can be selectively etched in between the active device layer and the substrate (Fig. 4a)[26,29–32]. For example, Al(Ga)As can be etched by hydrofluoric acid whereas (In)GaAs-based materials are resistant to hydrofluoric acid, allowing Al(Ga)As to be used as a sacrificial layer to create freestanding GaAs-based devices such as solar cells, LEDs and detectors[33–40]. Complex perovskite oxides use acid or water-soluble layers to produce freestanding single-crystalline films. For example, $La_{0.7}Sr_{0.3}MnO_3$ was used as a sacrificial layer to release centimetre-scale perovskite films in KOH, whereas Lu et al. demonstrated synthesis of freestanding thin-film heterostructures by engineering a water-soluble $Sr_3Al_2O_6$ buffer layer[41–45]. Although chemical lift-off of centimetre-scale coupon wafers is relatively quick, wafer-scale release typically takes several hours to even days[30,46], which limits throughput and is detrimental for high-volume production. Several groups have devised creative ways to accelerate the lift-off process by inducing epitaxial strain and adding physical weights to the exfoliated film to maximize the area of the sacrificial layer exposed to the etchant solution[47,48]. Roughening of the host substrate after the chemical etch is also an issue, preventing immediate reuse of the substrate since chemical and mechanical polishing is required to reconstruct an epi-ready surface. Although atomically smooth etching morphology has been demonstrated, significant reusability of the substrate (>50 times) has not been demonstrated to date[30]. Chemical lift-off has seen the most success in the photovoltaic industry, where world-record efficiencies have been demonstrated via a photon recycling effect by integrating the photovoltaic cell with a rear surface mirror[49].

Laser lift-off is a technique of separating epitaxial layers from transparent substrates such as sapphire or SiC using excimer lasers (Fig. 4b). This method uses a short-wavelength laser, which is absorbed by the GaN film, decomposing the substrate/GaN interface into metallic Ga and N_2 gas, which can then be heated above the melting point of Ga (30 °C) to separate the epilayer from the substrate. Damage-free separation of GaN from sapphire was demonstrated using a 248 nm laser at 400–600 mJ cm^{-2} fluences[50]. However, because of the induced plasma at the interface during laser excitation, the substrate surface is roughened, with roughness ranging from 60 to 90 nm (refs. [51,52]) such that subsequent epitaxy cannot be done unless the substrate is chemically and mechanically polished. This technique is fast and robust for epitaxial films that are grown on high-bandgap substrates, but therefore limited in terms of the scope of materials possible. Nevertheless, high-bandgap materials have been gaining increasing attention over the past few years for applications in quantum computing[53], power electronics[54–59] and high-efficiency laser diodes[60–62], which may potentially allow vertical integration of high-bandgap electronics and optoelectronics on a single platform.

Mechanical spalling is a brute force method of creating thin films in the micrometres-thick range, where a metal stressor layer (typically thick Ni films) is used to initiate a crack running parallel to the substrate (Fig. 4c). Mechanical spalling has been demonstrated for Si, Ge, GaAs and GaN substrates at IBM to generate thin-film CMOS circuits[63–65], solar cells[66–69] and LEDs[70,71]. As can be deduced from the process description, mechanical spalling is a relatively crude process that produces films with thicknesses in the hundreds of nanometres to several micrometres range and the roughness of

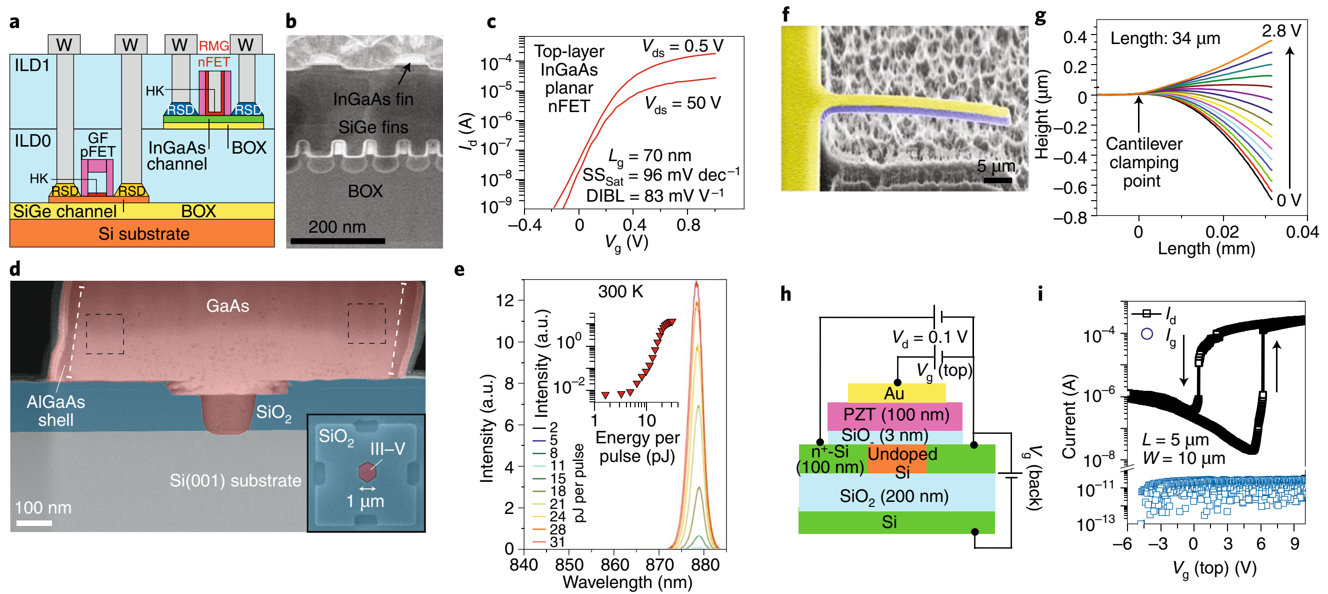


Fig. 5 | Demonstration of advanced heteroepitaxial techniques for heterogeneous integration of dissimilar materials onto silicon. a, Schematic of 3D monolithic integration of III–V finFETs on a SiGe finFET platform. ILD, interlayer oxide; RSD, raised source–drain; HK, high *k*; GF, gate-first; W, gate metal; RMG, replacement metal gate; BOX, buried oxide. **b**, Scanning transmission electron microscopy (STEM) image of InGaAs finFET epitaxially grown on a SiGe finFET platform. **c**, I_d–V_g characteristics of the InGaAs finFETs grown on a SiGe finFET template. I_d, drain current; V_g, gate voltage; V_{ds}, drain–source voltage; L_g, gate length; SS_{sat}, subthreshold slope; DIBL, drain-induced barrier lowering. **d**, Cross-sectional annular dark-field STEM image of AlGaAs/GaAs microdisk lasers grown on Si via TASE. **e**, Lasing characteristics of the AlGaAs/GaAs microdisk at room temperature. Inset: light-in light-out curve. **f**, SEM of single-crystalline PMN-PT cantilever on Si. **g**, Cantilever displacement as a function of applied voltage. **h**, Schematic diagram of a single-crystal PZT-gated Si FET. **i**, The I_d–V_g (top gate) characteristics of the FET shown in **h**, where an abrupt hysteresis shown demonstrates channel charge control by the transferred PZT layer. The black curve indicates the drain current (I_d) and the blue curve indicates gate current (I_g). *L* and *W* are length and width, respectively. Figure reproduced from: **a**, ref. [75], IEEE; **b**,**c**, ref. [74], Elsevier; **d**,**e**, ref. [76], American Chemical Soceity; **f**,**g**, ref. [77], AAAS; **h**,**i**, ref. [42], under a Creative Commons licence CC BY 4.0.

the substrate surface is the roughest compared with other epitaxial lift-off techniques. In addition, the spalling propagation depth cannot be precisely controlled and depends on the surface orientation[72]. Thus, this method could be used for vertical integration of electronic circuit stacks (for example, 3D very-large-scale integration) where physical coupling between each layer is not required.

The 2DLT technique utilizes the benefits of vdWE and remote epitaxy to generate freestanding single-crystalline membranes (Fig. 4d). This method is enabled by vdWE and remote epitaxy in unison with 2D material-assisted transfer techniques, where the weak vdW bonding of 2D materials facilitates exfoliation of epitaxially grown films from the substrate, leaving a pristine surface after exfoliation. This process is analogous to mechanical spalling, but has several advantages. First, the spalling depth is determined by the position of the 2D material rather than the stress of the metal stressor film and thus more controllable. Second, it requires much less stress compared with spalling and is easier to remove the metal after exfoliation. Third, the separation interface is atomically sharp due to the 2D buffer layer not allowing covalent bonds between the epilayer and the substrate. Thus, potentially, no wafer refurbish process is necessary, such as chemical and mechanical polishing. However, some challenges do still remain for industrial adoption of this technique. For example, elemental semiconductors such as silicon and germanium cannot be grown remote epitaxially due to the non-ionicity of their bonds[17]. Also, the area yield of exfoliation depends on the quality of the transferred graphene layer. If there are significant tears, holes or wrinkles after transferring graphene, both the material quality and the smoothness of the as-exfoliated substrate will be deteriorated.

For these layer-transfer techniques to be truly utilized at the industrial scale, wafer-scale transferability must be achieved. Chemical lift-off techniques have been demonstrated on 150 mm (6 inch) GaAs substrates with commercial thin-film flexible solar cell arrays available using 100 mm (4 inch) substrates by several companies (for example, SolAero Technologies, Microlink Devices). We note that the demonstrated thin-film solar cells use an InGaAs metamorphic graded buffer layer to grow low-defect, high-efficiency triple junction solar cells consisting of an $In_{0.3}Ga_{0.7}As$ bottom cell, GaAs middle cell and $In_{0.5}Ga_{0.5}P$ top cell with an AlAs sacrificial layer on a GaAs substrate[73]. Laser lift-off techniques have also shown their potential for full wafer-scale lift-off of GaN-based epitaxial device layers grown on sapphire substrates, with commercial equipment supporting up to 200 mm (8 inch) wafers. Mechanical spalling was also used to demonstrate wafer-scale (50 mm (2 inch)) thin-film device layers of Si, GaN and GaAs materials using Ni stressor metal[28,69–71]. However, 2DLT is, at the moment, a nascent technology and true wafer-scale (>50 mm) exfoliation and transfer is yet to be demonstrated. As mentioned above, precisely controlling the quality and defects of graphene at the wafer scale must be achieved first for 2DLT to be viable as a wafer-scale process.

Applications of advanced epitaxy and lift-off technology

The TASE method by IBM, which is an advanced selective growth technique using an oxide mask of sub-100 nm opening, has been utilized to demonstrate defect-free integration of a wide range of III–V devices on silicon CMOS. For example, a 3D monolithic integration of InGaAs wide-fin n-type field-effect transistor (nFET) devices were grown and fabricated on top of a SiGe-OI (on insulator) short-channel fin p-type FET (pFET) to realize state-of-the-art CMOS inverters operating at a supply voltage V_{DD} = 0.25 V (refs. [74,75]; Fig. 5a–c). AlGaAs/GaAs microdisk lasing at room temperature was also successfully demonstrated on silicon substrates, with

lasing thresholds around 2 pJ per pulse with a cavity size of 1 μm at a wavelength of 830 nm (ref. [76]; Fig. 5d,e). These demonstrations convincingly demonstrate the possibility of 3D integration of III–V and III–N devices on silicon-based platforms for monolithically stacked multilevel photonics and electronic circuits. Moreover, researchers were able to extend the material spectrum by integrating complex oxide films on silicon-based devices as well. For example, giant piezoelectric $Pb(Mg_{1/3}Nb_{2/3})O_3$–$PbTiO_3$ (PMN-PT) films were able to be grown on silicon by utilizing an $SrTiO_3$ buffer layer, allowing realization of a hyperactive microelectromechanical systems (MEMS) cantilever on silicon with large mechanical movements at very low voltages compared with bulk materials (Fig. 5f,g)[77]. A similar ferroelectric material, $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT), was also epitaxially grown and transferred onto a transistor to create a single-crystal PZT gated silicon transistor, allowing control of the channel charge via the polarization of the PZT layer (Fig. 5h,i)[42]. One of the early demonstrations of heterointegration of epitaxial thin films was achieved by Yablonovitch et al. through vdW bonding. The authors transferred thin semitransparent GaAs membranes created by chemical lift-off onto various substrates such as silicon, glass, sapphire, $LiNbO_3$, InP and diamond substrates[26,78]. A thin layer (<100 Å) of amorphous oxide was formed at the GaAs/substrate interface, showing the potential of heterogeneous integration of thin epitaxial films in the early 1990s. Following this research, epitaxial thin films have yielded many creative applications for functional electronic and optoelectronic devices such as photodetectors, solar cells, lasers and LEDs, especially on flexible and stretchable platforms.

Photodetectors on a thin-film substrate can be transformed into a conformal architecture, which allows a wide field of view and obtains low-aberration images with simple optical elements, mimicking biological imaging systems such as human and insect eyes[79–81]. Ko et al. demonstrated a hemispherical conformal imager based on a compressible silicon photodiode array with a single-element lens system[80]. Although the imager has only one lens to focus an image onto the focal plane array, high-quality images were obtained without off-axis optical aberration by matching the surface of the focal plane array to the calculated Petzval surface of the lens (Fig. 6a). For a more general approach to offer various wavelength detection with epitaxially grown active materials, a thin-film InGaAs photodetector array was fabricated via a chemical epitaxial lift-off process[81]. The flexible array, which is sensitive to near-infrared wavelength, was deformed into a convex cylindrically curved imager to achieve 2π field of view, and exhibited high performance even with a thin InGaAs active layer by virtue of having backside metal mirrors (Fig. 6b). While the conformal imager demonstrated was in a cylindrical shape, the epitaxial thin film has the potential to be deformed into a hemispherical shape via a concave mesh structure or a kirigami with proper design of cutting patterns.

A similar kirigami approach can be applied to solar cells fabricated out of a thin epitaxial film to realize a simple and low-cost solar tracking system, maximizing solar power generation over the course of a day without additional heavy, bulky components and structural supports[82]. Figure 6c shows the integrated thin-film crystalline GaAs solar cells fabricated by using chemical epitaxial lift-off and kirigami line cut patterning, exhibiting near single-axis tracking performance. Meanwhile, epitaxial lift-off has been used to achieve cost-competitive solar energy conversion via a wafer recycling process[32,40,83] and to fabricate a high-efficiency solar cell by mechanically stacking separately grown active materials[68,84–86].

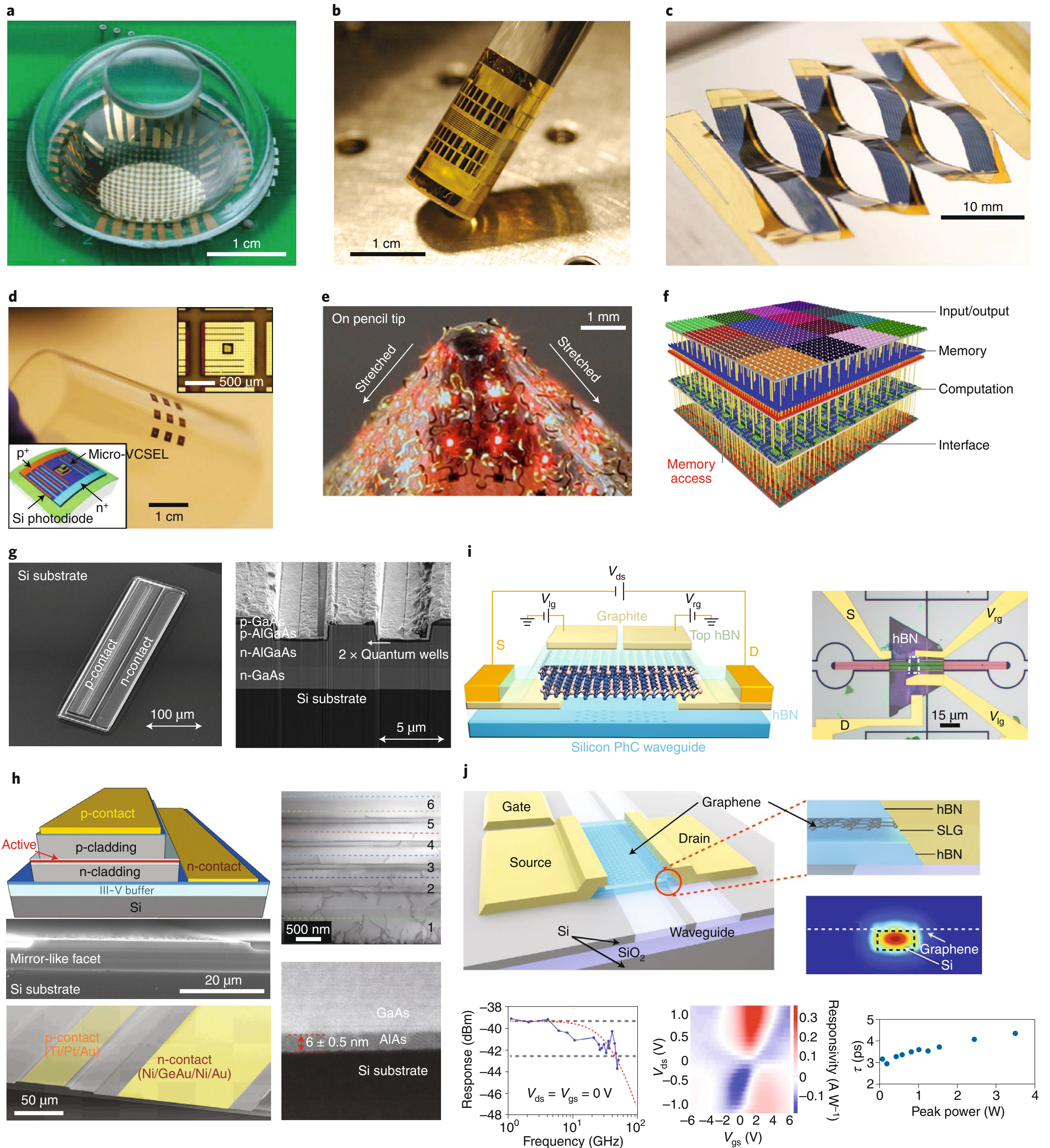
For laser applications, several driving forces have existed to let researchers use epitaxial lift-off to overcome limitations in current laser technology. The two main motivations for the use of epitaxial lift-off for laser systems are (1) flexible architectures to allow the laser to be integrated onto low-modulus and curvilinear surfaces such as biological tissues and skins for biomedical applications[87,88], and (2) heterogeneous integration with unusual combinations of materials and device structures such as integration of III–V photonic materials onto silicon-based conventional electronic backplane circuits or waveguides[89–91]. An example of the former is a vertical-cavity surface-emitting laser transferred onto a flexible plastic substrate by employing an epitaxial lift-off and transfer printing process (Fig. 6d)[88]; an example of the latter is heterogeneous integration of GaAs-based edge emitting lasers onto a silicon substrate for continuous-wave operation, representing a potential pathway to low-cost integration of III–V photonic devices and circuits on foreign substrates[90]. Eliminating the native substrate also enables other applications of LEDs, conceptually similar to the laser applications[92–96]. Figure 6e shows an example of inorganic InAlGaP red LEDs with non-coplanar serpentine bridges on a thin polydimethylsiloxane substrate[92], demonstrating its capability for robotics and clinical medicine applications.

In addition to optoelectronic device applications, epitaxial growth and lift-off have the potential to be exploited to realize non-von Neumann computing systems on a single chip by heterogeneously integrating the required components[97–99]. Computational complexity and memory consumption are continuously increasing along with advances in machine learning and artificial intelligence, while traditional CMOS scaling has reached the end of its technological limit. Subsequently, demand for alternative computing architectures, circuits, devices and materials is surging to improve the computation performance and energy efficiency of computing systems. One promising approach to mitigate the von Neumann

Fig. 6 | Demonstrations of advanced epitaxial lift-off and transfer techniques for heterogeneous integration of devices onto silicon. a, Photographic image of a hemispherical artificial eye utilizing arrays of small silicon photodetectors epitaxially lifted-off from its substrate. **b**, An 8×100 InGaAs photodiode array deformed into a convex form fabricated by chemical lift-off methods. **c**, Photograph of flexible GaAs films cut into kirigami structures, enabling near single-axis tracking performance. **d**, Images of micro-vertical-cavity surface-emitting lasers (VCSELs) on a polyethylene terephthalate substrate with a GaAs quantum well active layer. The inset on the top right shows a micrograph of the VCSEL device, while the inset on the bottom left shows a schematic diagram of the VCSEL device. **e**, Optical image of an array of InAlGaP red LEDs (6×6), tightly stretching onto the sharp tip of a pencil. **f**, Illustration of a heterogeneously integrated nanosystem. The bottom layer is silicon FET logic and the second layer consists of CNFET logic for the CNFET row decoders and CNFET classification accelerator. The third layer has 1 Mbit RRAM and CNFET sensors are on the top layer. The layers are connected through dense vertical interconnects. **g**, Tilt view and cross-sectional SEM image of GaAs-based laser transfer printed onto a silicon substrate. The fabrication is carried out after the epitaxial coupon is transferred. **h**, Schematic of a III–V GaAs laser monolithically grown on top of silicon using advanced epitaxial methods such as AlAs low-temperature (bottom right SEM) buffer layer and dislocation filtering superlattice layers (top right SEM). The coloured dashed lines indicate increasing strained superlattice layers. **i**, Schematic and micrograph of a $MoTe_2$ LED/photodetector integrated onto a silicon photonic-crystal waveguide. V_{lg}, left gate voltage; V_{rg}, right gate voltage; D, drain; S, source; PhC, photonic crystal. **j**, Schematic of a graphene photodetector encapsulated in hBN on a silicon photonic integrated circuit with outstanding bandwidth (bottom left), responsivity (bottom centre) and response time (bottom right). V_{gs}, gate–source voltage; SLG, single-layer graphene; τ, response time. Figure reproduced from: **a**, ref. [80], Springer Nature Ltd; **b**, ref. [81], American Chemical Society; **c**, ref. [82], under a Creative Commons licence CC BY 4.0; **d**, ref. [88], Wiley; **e**, ref. [92], Springer Nature Ltd; **f**, ref. [99], Springer Nature Ltd; **g**, ref. [90], Springer Nature Ltd; **h**, ref. [8], Springer Nature Ltd; **i**, ref. [101], Springer Nature Ltd; **j**, ref. [102], American Chemical Society.

bottleneck is moving to an on-chip memory-based computing system instead of a dynamic random access memory-based off-chip computing system[99]. Figure 6f shows a schematic of a 3D-integrated on-chip memory computing system for sensing and classifying gases, consisting of an input/output layer (carbon nanotube FETs (CNFETs)), a memory layer (resistive random access memory, RRAM) and a computation layer (silicon FETs and CNFETs). The integrated system can capture massive amounts of gases (data) in real time, store the data directly in RRAM and perform in situ classification of the gases in the computation layer.

The ultimate goal would be to utilize advanced epitaxial techniques together with layer-transfer technologies to integrate various highly efficient electronic and photonic components made of dissimilar materials onto a single wafer. Promising demonstrations have been made by coupling III–V optoelectronic devices or functional 2D layers onto silicon substrates. For example, state-of-the-art III–V lasers on silicon was demonstrated using a transfer printing method, where epitaxial GaAs stacks were grown, lifted-off from the substrate via sacrificial chemical etching and transferred using polydimethylsiloxane as a stamp onto the silicon substrate



(Fig. 6g)[90]. Similar success of integrating quantum dot III–V lasers on silicon was seen by using a low-temperature AlAs buffer layer and dislocation filtering layers (Fig. 6h)[8]. Furthermore, integrating 2D materials such as graphene and transition metal dichalcogenides onto foreign substrates has seen a recent surge of interest due to their novel and outstanding physical properties[100]. Recently, the transfer of $MoTe_2$, acting as both an LED and photodetector, onto a silicon photonic-crystal waveguide was demonstrated (Fig. 6i)[101], with similar success integrating graphene-based 2D photodetectors (graphene passivated in between hBN layers) on silicon photonic integrated circuits (Fig. 6j)[102]. We note that there are still challenges in epitaxial growth of perfectly uniform and reproducible 2D materials using conventional growth methods discussed in this Review due to the thermodynamic limitations of 2D materials. This may result in varying degrees of variation in the film or structure, such as thickness, doping level and crystal orientation. New methods to control these variations as well as processes to work around this challenge are being developed and reported continuously[103–107]. With substantial progress in transferring wafer-scale 2D materials[107], these recent advances in heterointegration of thin-film III–V, III–N and 2D materials promise an unprecedented platform for non-silicon-based electronic and photonic devices to be integrated with current state-of-the-art silicon-based technologies.

Outlook

In the short term, growing device-quality epitaxial layers on silicon wafers for monolithic integration of vertically stacked multifunctional integrated circuits will significantly reduce integrated circuit footprints. It will also allow all-in-one chip platforms to be created that couple photonic circuitry with state-of-the-art sensors, transistors and memory elements being actively processed by neuromorphic chips[108]. Such a platform can be used as a universal processor for the Internet of Things and the recently emerging Artificial Intelligence of Things. For this to happen, however, several other technological advancements must be made in parallel, such as vertical interconnecting schemes, fabrication process compatibility, efficient heat distribution/dissipation and layout design, such that all the individual layers are well coupled without interfering with each other.

While monolithic integration with advanced epitaxy techniques can be the simplest way of coupling different materials, the material quality of epitaxial films grown by heteroepitaxy is still not ideal. As an alternative approach, various lift-off techniques for heterointegration have been developed to produce defect-free epitaxial layers on lattice-matched substrates followed by release of the layers from the substrate. To secure cost-effective heterointegration of various freestanding membranes, at least, the cost required for lift-off must be lower than that for substrates by maximizing substrate reusability. While various lift-off techniques developed so far have shown promising preliminary devices, they have not satisfied requirements needed to match the large-volume manufacturing at a scale seen for current integrated circuit industries. We believe that a high-throughput lift-off process may be secured by further development of the 2DLT technique as it offers fast release of epilayers at controllable interfaces. However, the quality of materials grown by remote epitaxy on graphene is not as matured compared with that obtained by conventional homoepitaxy, which must be addressed in future work.

Owing to their ability to produce thin single-crystalline freestanding flexible membranes, epitaxial lift-off techniques could, with further development, meet the requirements of flexible, conformal and multifunctional electronics for applications in the Internet of Things, smart cities, smart vehicles and wearable electronics. Together with monolithic integration by heteroepitaxy, heterointegration by lift-off could eventually allow the mix and match of various thin-film membranes, which are stacked-up to create advanced heterointegrated systems. While 2D material-based heterostructures have received significant attention so far due to their stackability, the electrical and optical properties of 2D materials are inferior to conventional semiconductor materials (3D materials). Thus, the stackability of various 3D materials enabled by advanced lift-off techniques could provide new opportunities for future electronics. Developments in 2D heterostructures can also play a role, as the 2D materials expand the materials that can be stacked with 3D material freestanding membranes.

There are many opportunities for epitaxial and layer-transfer techniques to enhance and broaden the current electronics industry. With the advancement of epitaxy on atomically thin 2D materials and layer-transfer techniques, epitaxial layers free from the lattice mismatch constraint are coming closer to reality, opening up new possibilities of integrating multilevel stacks of heterogeneous crystalline semiconductor, oxide and 2D materials. We speculate that, eventually, trying to find a suitable and expensive substrate to grow defect-free single-crystalline layers will become a thing of the past. Progress in heteroepitaxy techniques will lead to innovations in the electronics industry, and lead to faster, smaller, lighter and more efficient devices with reduced production costs.

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Author contributions

H.Kum, K.L., and J.K. conceived the project. All authors contributed to the writing of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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