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REVIEW PAPER

Copper Bonding Technology in Heterogeneous Integration

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Abstract

As semiconductor device scaling faces a severe technical bottleneck, vertical die stacking technologies have been developed to obtain high performance, high density, low latency, cost effectiveness and a small form factor. This stacking technology is receiving great attention from industry as a core technology from the point of view of recent heterogeneous integration technology. Most importantly, bonding using copper is aggressively studied to stack various wafers or dies and realize genuine three-dimensional packaging. Copper is emerging as the most attractive bonding material due to its fine-pitch patternability and high electrical performance with a CMOS-friendly process. Unfortunately, copper is quickly oxidized, and a high bonding temperature is required for complete Cu bonding, which greatly exceeds the thermal budget for the packaging process. Additionally, the size of Cu pads is decreasing to increase the density of interconnections. Therefore, various copper bonding methods have been studied to realize copper oxidation prevention, a low bonding temperature, and a fine-pitch Cu pad structure with a high density. Furthermore, recently, hybrid bonding, which refers to the simultaneous bonding of copper pads and surrounding dielectrics, has been considered a possible solution for advanced bonding technology. This paper reviews recent studies on various copper bonding technologies, including Cu/oxide hybrid bonding.

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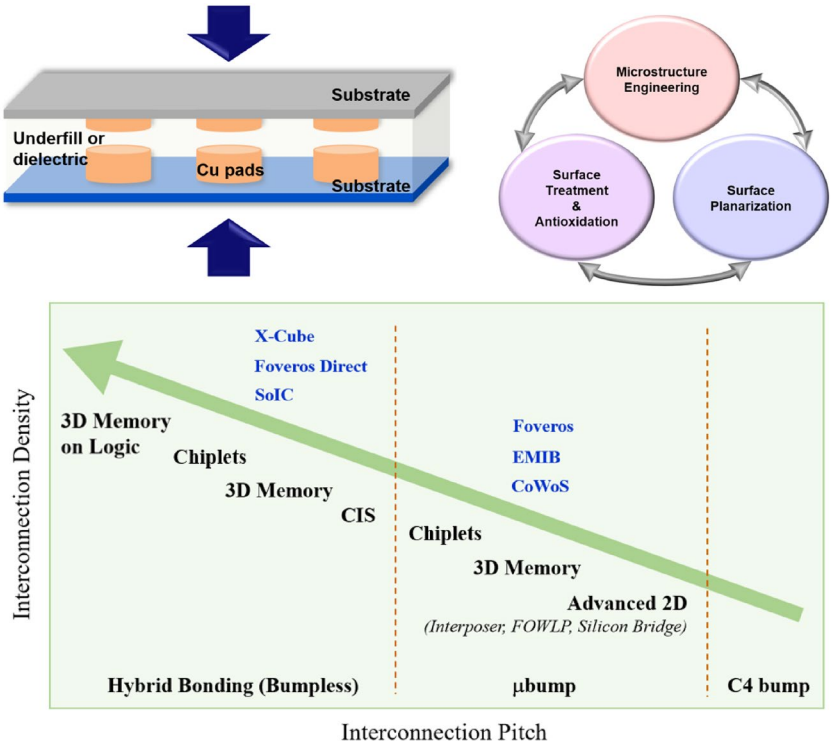
Graphical Abstract



Keywords Cu bonding · Hybrid bonding · 3D packaging · Heterogeneous integration · Antioxidation

1 Introduction

Until recently, the scaling down of transistors has continued under Moore's law, which predicts that the number of transistors on integrated circuit (IC) chips will double almost every two years to continuously improve the figures of merit of the chips, such as performance, power efficiency, and cost. However, severe challenges such as the physical limit of scaling, material, thermal management and cost issues are being encountered and have yet to be overcome [1–4]. To make a breakthrough and keep attaining the benefits associated with Moore's law, advanced integration, also known as heterogeneous integration (HI), including three-dimensional (3D) packaging and system-in-packaging (SiP), is proposed as a powerful alternative method. From the viewpoint of a system of IC chips rather than a chip itself, HI with a new architecture of IC chips can bridge the technology gap between transistors and conventional packaging. In addition, the world of electronic device packaging is rapidly changing. Recent trends in electronic devices such as artificial intelligence (AI), internet of things (IoT), and 5G are also boosting HI, such as fan-out wafer-level packaging (FOWLP), redistribution layer (RDL) interposers, Si interposers, Si bridges, 3D die or wafer packaging, and chiplet integration. All of these realizations have in common the need for greater miniaturization, high-performance computing, fine-pitch interconnects, and high density at the packaging level. Indeed, HI has become the key technology trend for advanced packaging since the end of the international technology roadmap for semiconductors (ITRS) in 2016.

Among advanced packaging technologies, 3D packaging is known to be a key method for future HI technology. Core processes for implementing 3D packaging include a through silicon via (TSV) fabrication process, a wafer grinding process, and a die or wafer bonding process [5–13]. Among them, die or wafer bonding technology is essential to physically stack devices three-dimensionally. Methods for bonding devices vertically include wafer-to-wafer bonding, die-to-die bonding, and die-to-wafer bonding. The device arrangement during stacking is divided into face-to-face bonding and face-to-back bonding. Processes include metal-to-metal bonding, oxide-to-oxide bonding, polymer-to-polymer bonding, and hybrid bonding that bonds a metal and a dielectric at the same time. Generally, metal-to-metal bonding has good thermal and mechanical reliability as well as excellent electrical properties, making it a suitable process for device stacking. However, the increasing density of input/output (I/O)

pins has decreased the bump pitch, making the use of conventional microbumps and underfills difficult. Solder-based bumps cannot afford a reduced I/O pitch of under 40 μm due to solder extrusion, collapse, and intermetallic compound (IMC) formation with scaled pitch [14, 15]. The degraded thermal conductivity of the underfill material also makes the devices vulnerable to thermal dissipation [16].

This difficulty can be overcome by the use of direct Cu-to-Cu bonding because copper, a metal commonly used for interconnecting chips due to its low resistivity, can be bonded by direct contact with itself in principle. Cu-to-Cu bonding can accommodate extremely high-density interconnections for high I/O pin numbers and increased power efficiency with small pitches of less than 20 μm [15, 17], hence receiving attention for the next-generation stacked packaging structure [11–13, 18, 19]. Device industry companies, including Sony, TSMC, Intel, Samsung and SK hynix, are very interested in a reliable and commercial method for Cu-to-Cu bonding down to the μm size [13]. However, there are few inclusive reports on 3D HI, although vertical interconnection is crucial to realizing HI. Therefore, it is necessary to comprehensively review representative studies for copper bonding technology from early works to recent advances. In this paper, various Cu-to-Cu bonding methods from thermal compression bonding (TCB) [20–22], the most straightforward method, to recent Cu/dielectric hybrid bonding [23–34] are studied. TCB is known to be effective, fast and profitable, while Cu hybrid bonding has been shown to be suitable for the mass-production processes of CMOS devices and has high potential for use as a next-generation vertical stacking packaging process. The basic mechanism of TCB is to induce the diffusion of Cu atoms at two different Cu interfaces, generally by using elevated temperature and pressure. Material engineering, such as modifying the residual stress or microstructure of Cu films and introducing other materials, such as non-Cu metals or alloys, are also widely studied methods. In Cu/dielectric hybrid bonding, bonding between dielectrics should be considered in addition to bonding between Cu pads. Process parameters, including chemical mechanical polishing, wafer/die cleaning, and wafer dicing, significantly affect the bonding results; therefore, the effects of bonding processes should be investigated and optimized. This paper mainly focused on summarizing various methods for TCB and hybrid bonding and understanding the bonding mechanism and its effect on bonding results for each method. Perspectives and challenges for future copper bonding technology are also organized in the latter part of the paper. This paper provides insight into extending and establishing bonding technology for 3D packaging in HI.

2 Direct Cu-to-Cu Bonding

Direct Cu-to-Cu bonding can occur simply by placing two copper surfaces together and allowing atoms to diffuse through the surfaces and construct a common lattice across the surface. However, this behavior is difficult to realize in practice, especially at room temperature and atmospheric pressure, since copper diffusion is slow at room temperature. Moreover, copper reacts with oxygen and quickly forms a copper oxide (one nm on bare Cu under ambient conditions in one hour [35]), which further prevents the diffusion of copper atoms. Therefore, direct Cu-to-Cu bonding requires a high temperature above 400 °C and a high pressure, which is known as TCB. In the TCB process, shown in Fig. 1a, the bonding temperature is the most important factor in Cu-to-Cu bonding, as the higher the bonding temperature is, the better the bonding interface because the diffusion rate exponentially increases with temperature in general [22]. It was also confirmed by an earlier experiment that a higher bonding temperature or longer annealing time improved the quality of bonding due to enhanced diffusion and grain growth [36]. However, there is a limited thermal budget when packaging many other devices, although elevating the bonding temperature is the easiest way to realize Cu-to-Cu bonding. Generally, bonding temperatures of up to 250 °C or 400 °C can be allowed when stacking dynamic random-access memory (DRAM) or not-and (NAND) flash memory, respectively, whereas logic devices such as microprocessors are limited to a thermal budget below 350 °C. The maximum bonding temperature would be limited by the certain packaging component that has the lowest allowable heat treatment temperature, and it would be more restricted for HI given that HI can be achieved by integrating a variety of electronic device components to operate appropriately for the intended purpose.

The removal of copper oxide and thus activation of the copper surface are also crucial to direct Cu-to-Cu bonding. Hence, the bonding pressure is an important factor to breakdown any copper oxides that may have formed, but it has to be as low as possible to avoid any mechanical failure in the whole packaging. There are several more factors to consider when applying direct Cu-to-Cu bonding to device packaging. The microstructure and texture of copper also affect Cu-to-Cu bonding because the diffusion of copper atoms is also dependent on the surface orientation of the copper [22, 37, 38]. Another key requirement for good TCB is surface planarization. Excellent planarity is mainly achieved by chemical mechanical polishing (CMP) with a chemically activated slurry [39]. CMP can flatten the surface to a roughness of a few nanometers and is one of the key factors for incoming wafers. In any case, the

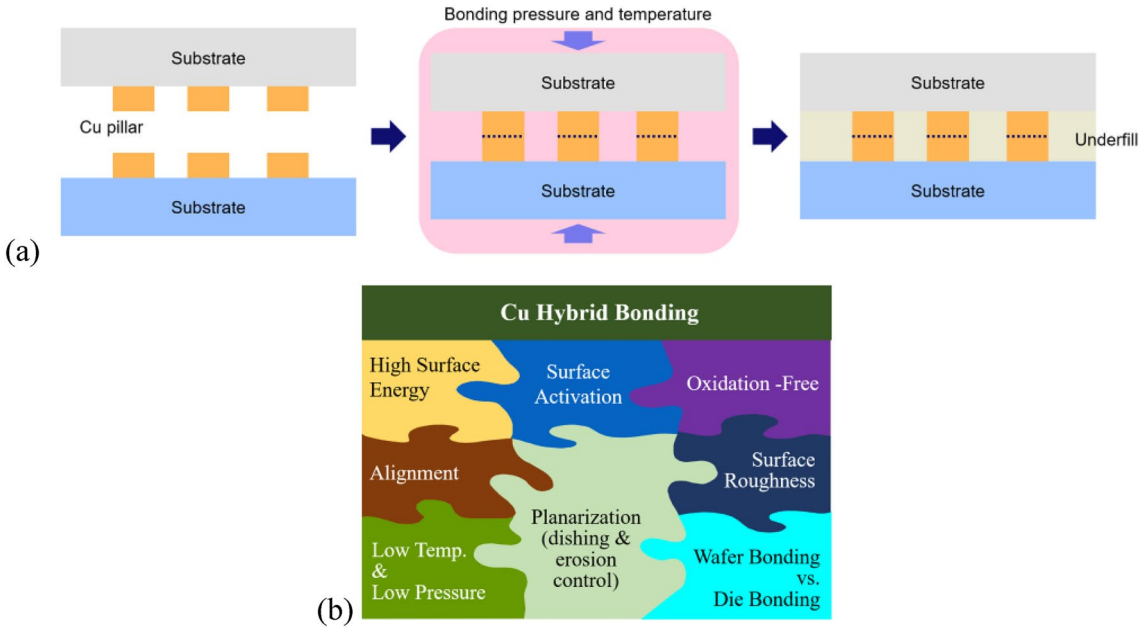


Fig. 1 **a** Schematic process flow of direct Cu-to-Cu bonding. **b** Key factors to consider in Cu bonding

entire bonding process and materials should be compatible with the standard environment of the semiconductor industry and should not damage any components or chips already fabricated in front-end-of-line (FEOL) and back-end-of-line (BEOL) processes. Overall, various key factors to consider in the Cu bonding process are presented in Fig. 1b.

Cu bonding technology was initially suggested from the late 1990s to early 2000s by a few groups, including RPI [40–42] and MIT [43, 44]. RPI mainly focuses on wafer bonding using a benzocyclobutene (BCB) glue layer with subsequent processes of deep etching and filling. MIT reported a bonding method in which via was etched and filled prior to wafer bonding, followed by TCB for wafer bonding at 400 °C for 30 min. Since the cornerstone of Cu bonding technology was established, many studies have been conducted to further develop bonding technology. In the following sections, various methods to directly bond Cu pads will be discussed. They can be divided into two categories based on whether they use the diffusion behavior of Cu (intrinsic Cu-to-Cu bonding method) or exploit extrinsic treatments to achieve effective bonding (extrinsic Cu-to-Cu bonding method), such as plasma treatment, nonplasma treatment and passivation with another metal layer. There are also other extrinsic methods using adhesive epoxy, nanoparticles and structural modification.

2.1 Modulating the Intrinsic Diffusion Behavior

The basic mechanism of Cu-to-Cu bonding is solid-state bonding through diffusion. Diffusion is driven by the random thermal motion of atoms and is greatly accelerated by density differences. Mechanisms for increasing density differences or, effectively the same thing, introducing stress into the metal lattices are described in this section. Density differences across the Cu-to-Cu interface where both surfaces are sputtered can be induced by using different voltages in the sputtering process. The same phenomenon can occur if the copper surface is simply bombarded by argon ions. The Cu lattice near the surface becomes disorganized and less or more dense than the Cu in the bulk depending on the accelerating voltage of the argon ions. Studies [26, 45, 46] on this idea varied the stress across the two interfaces by changing the acceleration with which the argon ions hit the Cu surface in the sputtering process. They found the maximum tensile stress in sputtered Cu when the argon pressure was 12 mTorr and the maximum compressive stress when the argon pressure was 3 mTorr. Making one side with the maximum compressive stress and the other side with the maximum tensile stress allowed TCB below 100 °C with a pressure of 0.25 MPa, and the sample showed a bond strength of 120 MPa [45].

Copper has a face-centered cubic structure in which the (111) surface has the greatest density of atoms. Diffusion

along the (111) plane on a Cu surface is several orders of magnitude higher than that along planes with other orientations. Realization of the (111) crystal orientation of copper is being actively investigated as a method to increase copper diffusion at low temperatures [22, 37, 38, 47, 48]. A simple creep model to describe fast surface diffusivity on the (111) Cu surface was recently proposed by Liu et al. [48]. Additionally, nanotwinned Cu has been reported to be more beneficial than polycrystalline Cu since the bonding interface with nanotwinned Cu showed a lower density and a smaller size of interfacial voids [47]. Shie et al. [37] reported Cu-to-Cu direct bonding at 300 °C with <111> -oriented nanotwinned Cu bumps in ambient N_2. Figure 2a shows a cross-sectional image of nanotwinned Cu bumps with columnar grains. The orientation of the Cu bump surface was obtained by electron backscatter diffraction (EBSD) and is shown in Fig. 2b. The bond showed a nearly void-free interface and a low bump resistance of 4.9 mΩ, but the shear strength value has not been reported.

2.2 Incorporating Extrinsic Methods for Cu-to-Cu Bonding

2.2.1 Using Plasma Treatment

Removing a copper oxide and inducing interdiffusion of copper atoms on the surface is the basic mechanism of Cu-to-Cu bonding, as described above. An activated copper surface can easily bond with a similar surface, facilitating copper diffusion from one to the other. Plasma treatment with forming gas plasma [49] or argon plasma [50] is a widely considered method to activate the copper surface and remove any thin layer of copper oxide. A room-temperature bonding method, the surface activated bonding method [51], removes oxide from the copper surface and activates the surface using argon plasma before bonding in ultrahigh vacuum. Activation of the surface with argon plasma can be performed by increasing subsurface hardening and creating compressive stress, which increases copper diffusion toward the unstressed area close to the bonding interface [50]. However, argon plasma bombardment can increase the surface roughness and degrade the bonding interface quality.

The formation of Cu nitrides with argon and nitrogen plasma is another approach to Cu-to-Cu bonding. A copper surface exposed to air readily forms oxides (Cu_2O, CuO), hydroxides ($Cu(OH)_2$) and carbonates ($CuCO_3$), all of which hinder bonding. Copper nitrate passivates the surface by preventing the formation of these compounds and is useful in Cu-to-Cu bonding because heat decomposes it into metallic Cu and nitrogen. Decomposition typically occurs at 300 °C but can occur at temperatures ranging from 100 to 470 °C, depending on the deposition and growth methods [19, 31]. Moreover, Cu_4N and Cu_3N have been reported to tend to offer metallic behavior and semiconducting behavior, respectively, unlike copper oxides [52]. Among copper nitrides such as Cu_3N and Cu_4N, Cu_4N is preferred because it has a lower resistivity and a lower decomposition temperature than Cu_3N [53].

An Ar/N_2 mixed plasma treatment has been reported to form passivating Cu_xN_y [54, 55] with improved bonding interface quality. According to Tan et al. [54], the two Ar/N_2 mixed plasma-activated Cu surfaces that are bonded and annealed at 300 °C for 2 h in a N_2 environment produce a resulting bond with a shear strength of between 15 and 20 MPa and low electrical resistance. When a mixed gas plasma is used, a uniform passivation layer thickness or stoichiometry may not be formed due to the constant collision of Ar ions in the plasma. As shown in Fig. 3a, a sequential plasma treatment method was proposed [18, 19], in which a noble Ar plasma is initially used to blast any copper oxide off of the surface, followed by a nitrogen plasma that forms copper nitride on the surface to prevent any return of the copper oxide. A lower RF power is the most effective for forming uniform Cu nitride (Cu_4N) passivation because of the lower plasma density. The mechanism by which the nitride passivates the copper surface, mostly by forming

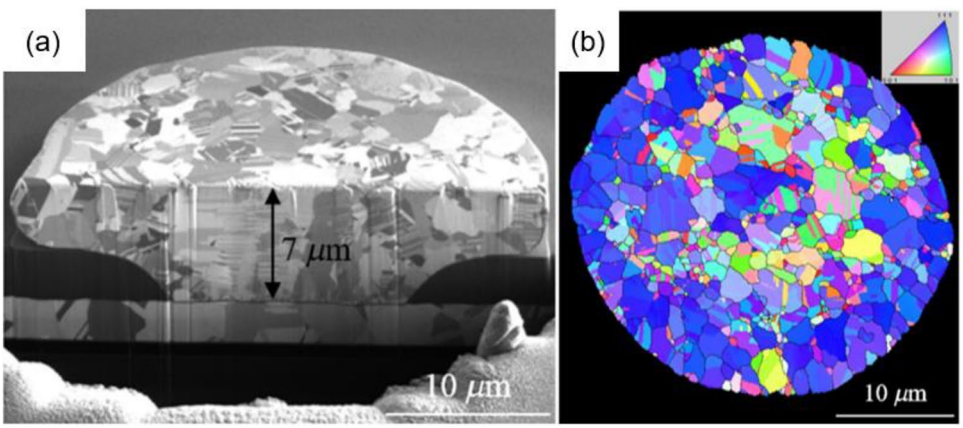


Fig. 2 **a** Microstructure of nanotwinned Cu bumps analyzed with a focused ion beam (FIB). **b** EBSD mapping of the surface orientation of the Cu bump. The (111) orientation is colored blue (reproduced from [37], Copyright (2019) The Japan Society of Applied Physics)

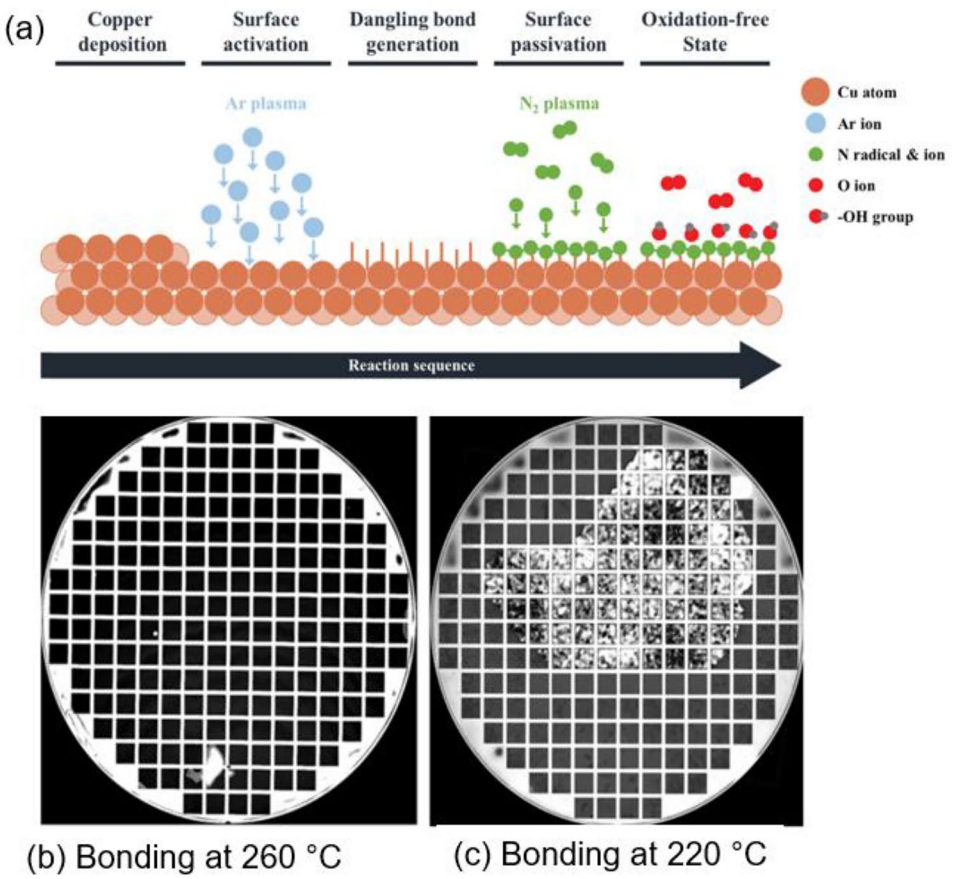


Fig. 3 Cu bonding using Ar/N_2 two-step plasma treatment: **a** Overall mechanism, and **b** bonding result at 260 °C and **c** 220 °C (reproduced from [56])

Cu_4N, is described by Park et al. [18]. The two-step plasma treatment eliminates the uneven native copper oxides on the copper and forms an ultrathin, even layer of copper nitride that prevents oxidation in air [19]. Park et al. [56] reported Cu–to-Cu bonding at 260 °C with a pressure of 0.9 MPa for 1 h using two-step plasma treatment and obtained a shear strength of ~ 62 MPa. Figure 3b, c show scanning acoustic tomography (SAT) images of Cu bonding using Ar/N_2 two-step plasma treatment at 220 °C and 260 °C. Copper nitride did not fully decompose at 220 °C, resulting in unbonded or weakly bonded regions compared to the fully decomposed and well bonded copper nitride in 260 °C bonding.

2.2.2 Using Nonplasma Treatment

Several alternatives to plasma surface activation have been tried, including various chemical treatments and xenon flash laser application. Surface cleaning is performed in a number of different ways and usually involves the removal of any copper oxide that might have grown on the copper surface using a mild acid. Copper oxide can be removed by wet chemical treatments such as buffered oxide etch (BOE) and sulfuric acid treatment [57]. Formic acid vapor [35, 58] was suggested to clean the copper surface because it removes copper oxides and produces a thin layer of copper formate in less than ten seconds. The formate can be decomposed into carbon dioxide and hydrogen by heating above 200 °C. Jangam et al. [35] reported that when using a formic acid vapor treatment, a shear strength of 150 MPa was obtained by bonding for 5 s at 240 °C. The ion-milled cross-sectional image of the Cu–Cu interface bonded by using formic acid vapor is shown in Fig. 4a. Peng et al. [59] reported a solvothermal treatment of copper in the presence of sodium formate, which led to crystallographic reconstruction of the copper surface into the (110) plane to a thickness of 200 nm to accommodate the hydrides. Oxides are excluded because the subsurface Cu atoms are fully bonded by O_2- and OH– groups. The xenon flash laser method [60] is based on the observation that hardening the surface increases the diffusion rate. A harder surface has a greater residual stress, which 'boosts' diffusion through the surface. Ten pulses of the xenon flash laser were used on the copper surface to both clear the oxide and activate the surface. Bonding at 250 °C for five minutes in a nitrogen environment immediately after the flash laser treatment gave a shear strength of 31 MPa. The resultant cross section of the bonding interface is shown in Fig. 4b. However, use of the laser is not very simple and does not appear to be popular.

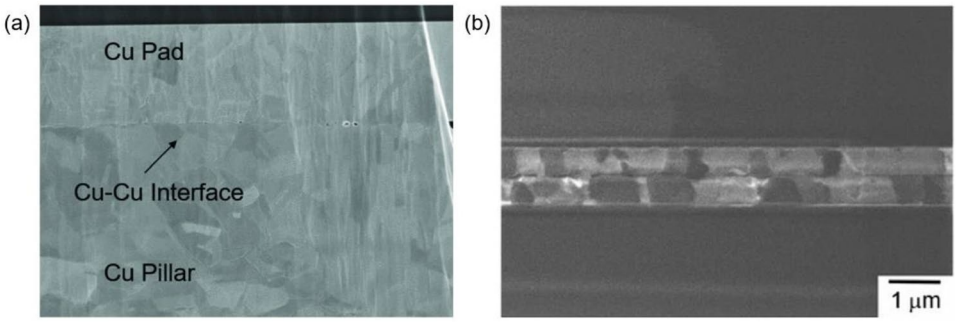


Fig. 4 Cu–Cu bonding interface obtained using **a** formic acid vapor [35] and **b** a xenon flash laser [60]

2.2.3 Using a Passivation Layer on the Copper Surface

Another method to obtain low-temperature Cu direct bonding is to use various passivation layers on the surface of Cu to prevent surface oxidation. First, a self-assembled monolayer (SAM) method [61–64] is a method in which a thin layer of alkane-thiol is deposited on the copper surface, where it protects against oxidation. The surface oxide has to be removed prior to application of the alkane-thiol, and since the alkane-thiol film decomposes at 250 °C, the bonding temperature has to be close to 250 °C for complete desorption. Tan et al. [63] reported Cu bonding at 250 °C with

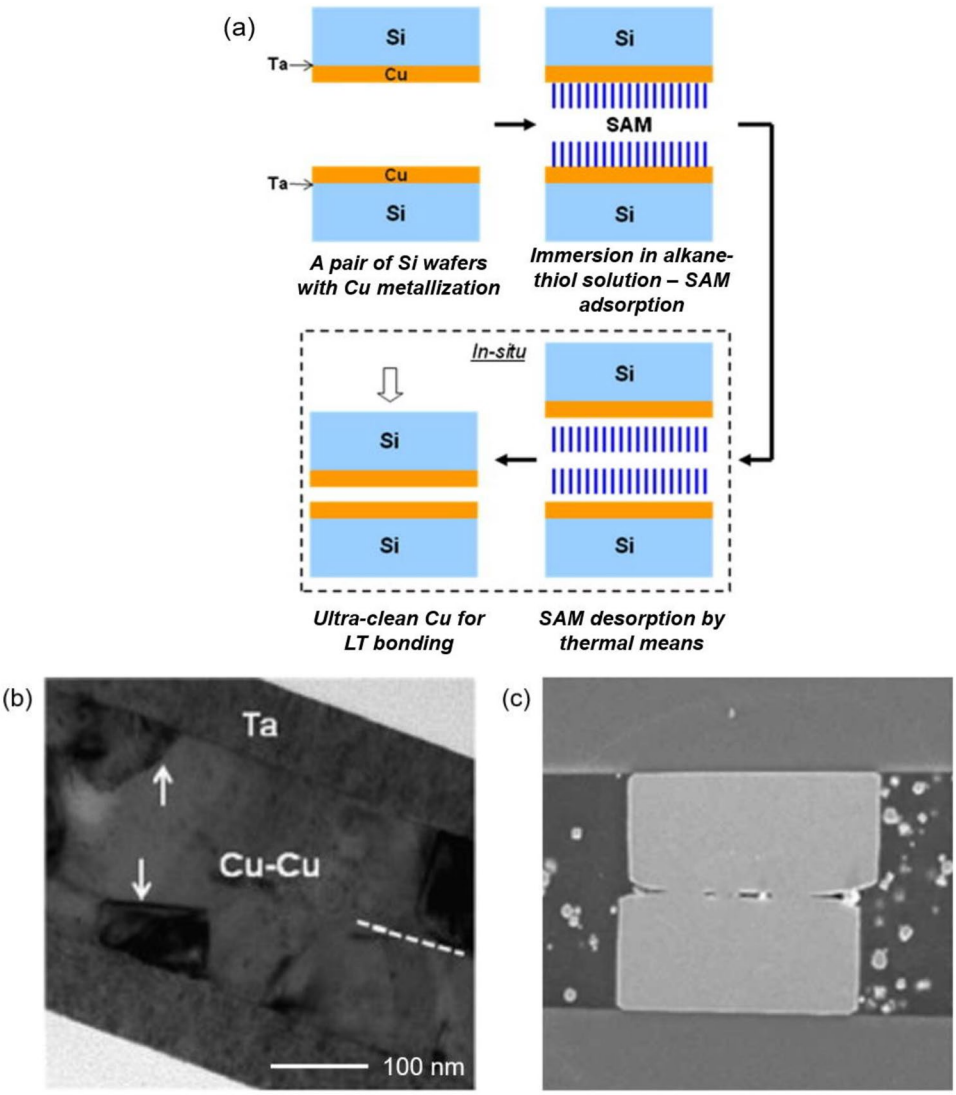


Fig. 5 **a** Summary of the process flow of SAM passivation to provide clean Cu surfaces [63]. **b** Grain growth across the bonding interface is observed (reproduced from [63]). **c** Scanning electron microscopy (SEM) image of the bonding interface obtained using conductive epoxy with Ni nanoparticles with a bonding pressure of 0.3 N/bump [65]

temporary passivation of an SAM and showed a > 60 MPa shear strength. The schematic process flow and the surface of Cu passivated with a SAM after bonding are presented in Fig. 5a, b, respectively. However, some compatibility issues with the semiconductor process are believed to arise because the SAM may remain at the copper interface and decomposed SAM residues may be present in the process chamber.

A conductive adhesive epoxy that contains nickel particles [65] can also be used in low-temperature Cu bonding applications. The surfaces to be bonded consist, on at least one side, of copper pillars or bumps. The epoxy, with its nickel, is spread between the two surfaces and cured. As part of the curing process, the epoxy shrinks and presses the surfaces together, trapping conductive nickel particles between the tops of the pillars and the other side. External pressure is applied during the curing process. Bonding was accomplished at 150 °C with an external force of 0.3 N/bump. However, some voids existed at the bonding interface, and some Ni particles were pressed out of the bonding interface. Unfortunately, neither the shear strength nor the conductivity were reported.

Unlike pure bulk Cu, which has a melting temperature of 1083 °C, Cu nanoparticles can melt below the bulk melting temperature. Several researchers [66–69] have suggested that the problem of bonding small pitch (< 10 nm) copper bumps could be overcome by using Cu nanoparticles. However, the difficulty of sintering with copper nanoparticles is that small nanoparticles, those with diameters < 5 nm, are quickly oxidized in air. Larger nanoparticles, with diameters > 30 nm, are not easily oxidized but are also not easily sintered. Luckily, larger nanoparticles usually have smaller ones on their surface, forming nanoagglomerates that are not all oxidized [66]. Other nanoparticles, such as Ag, can be used in Cu-to-Cu bonding [70, 71]. Silver nanoparticles can be deposited in the form of a loose surface layer. A tangle of nanoparticles is formed that looks and acts as a kind of Velcro. Two such surfaces can be pressed together and immediately form a weak bond. Once joined, they can be heated, and the nanoparticles sinter, together with the large agglomerates, to form a good bond. Given examples include an initial bond at 180 °C with a pressure of 50 MPa for 5 min followed by annealing for 25 min at 200 °C. However, the bonding pressure should be over 50 MPa in this work to achieve a successful bonding interface, at which plastic deformation of Ag nanoparticles can occur. Otherwise, nanovoids would occur at the bonding interface. Wang et al. [72] and Zhang et al. [73] used novel citrate-coated nanosized silver pastes to form robust Cu–Cu bonding under ambient air. They synthesized citrate-coated silver nanoparticles with an average diameter of 4.76 nm by using a sodium citrate ($Na_3C_6H_5O_7$) solution and silver nitrate ($AgNO_e$) solution. The effects of bonding temperature (180–280 °C), bonding time (0–60 min) and bonding pressure (0–10 MPa) were investigated to characterize bonding strength. The maximum bonding strength for each bonding parameter was reported at 260 °C, 60 min, and 10 MPa. It is noted that bonding strength slightly decreased at 280 °C due to a weakened plastic flow of the joint at the temperature. The optimized process conditions were found to be a bonding temperature of 260 °C, a bonding time of 30 min, and a bonding pressure of 1 MPa, and a shear strength of 27.5 MPa. They also reproduced the excellent thermal stability of the Cu joints at 150 °C.

As mentioned above, pure clean copper surfaces require temperatures of over 400 °C to form complete bonds. To reduce the bonding temperature, thin layers of metal rather than nanoparticles on copper, such as Ti [74–76], Au [77], Pd [78], Pt [79], and Ag [80, 81], have been studied. Their applications share the common aims of preventing copper oxide growth and forming a strong conductive joint at a relatively low temperature. They also share a common working mechanism, as shown in Fig. 6a. The copper diffuses through the metal film, meets the copper that has diffused on the other side and builds a common lattice that forms a strong bond.

Huang et al. [82] and Panigrahi et al. [74, 76] reported on the use of titanium (Ti) in copper bonding. There are several difficulties with the use of Ti. It oxidizes in air and diffuses into the bulk copper. At a thickness less than 3–4 nm, it does not prevent oxides from forming on the copper, while at a greater thickness, the Ti impedes the interdiffusion of the copper atoms through the titanium. Nevertheless, successful copper bonding with a shear strength of 190 MPa was reported with an optimal titanium thickness of 3 nm, bonding temperature of 175 °C and bonding pressure of 0.25 MPa. A thicker Ti film may be used in conjunction with pressure. Park et al. [75] formed a good bond with a shear strength of 30 MPa using 12 nm titanium. The bonding was performed at 200 °C with a pressure of 30 MPa for 1 h. Since Ti oxide can increase the contact resistance of the bonding structure, the diffusion of broken Ti oxide nanolayers into Cu must be studied or metals without oxide formation must be evaluated. Bonam et al. [77] reported that a 2 nm gold (Au) film produced copper bonding at 140 °C with a > 200 MPa shear strength. Gold simultaneously prevents surface oxidation and enhances diffusion. Huang et al. [78] reported that a 10 nm film of palladium (Pd) allowed copper bonding at 150 °C and showed that the specific contact resistance remained stable at approximately 10^{-6} Ω-cm^2 after 168 h of unbiased highly accelerated stress test (HAST) operation. The copper diffused through the Pd thin film faster than through bulk palladium. The transmission electron microscopy (TEM)-energy-dispersive X-ray spectroscopy (EDS) line profile result after bonding with a thin Pd layer is shown in Fig. 6b, which coincides with the proposed mechanism of metal passivation. The use of

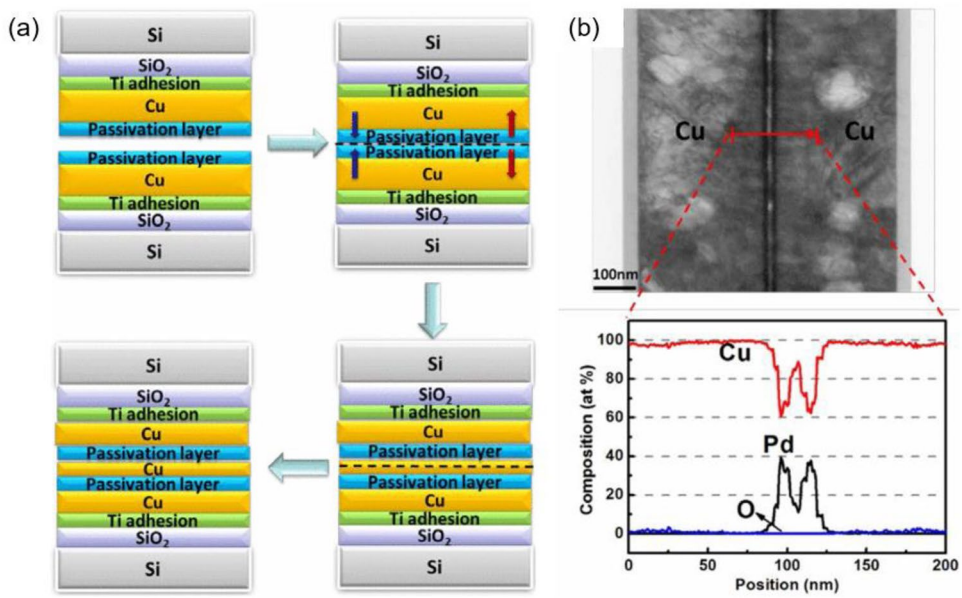


Fig. 6 **a** Schematic diagram of the working mechanisms in metal passivation methods. **b** TEM-EDS line scan profile of the Cu/Pd–Pd/Cu bonded structure. It clearly shows that Cu diffused through the Pd thin film (reproduced from [78])

a platinum (Pt) film has been reported by Liu et al. [79], who found that bonding at 200 °C for 3 min under a regular atmosphere gave a bond strength of 8.2 MPa. Silver (Ag) is also a good candidate as a passivation metal because it is a good conductor, and any silver oxide is removed by a hydrogen-based plasma before bonding. Kim et al. [80] reported the use of a 15 nm silver film in copper bonding at 180 °C with a pressure of 30 MPa for 30 min and showed a shear strength of ~ 14 MPa. This study showed that some of the Ag layer remained at the bonding interface due to 30 min of bonding without an annealing process. Figure 7 shows the annealing effect in Cu–Cu bonding using an Ag nanolayer. With annealing at 200 °C, complete Cu diffusion into the bonding interface and good Cu–Cu bonding are observed, but without annealing, the Ag layer remains at the bonding interface, and nonuniform Cu bonding is observed. Chen et al. [81] reported the use of a 30 nm silver (Ag) film in copper bonding at 180 °C with 90 MPa for 3 min in a regular atmosphere. They found that a Ag layer with a smaller grain size has more paths for Cu diffusion and that the diffusivity from Cu to Ag is higher than the diffusivity from Ag to Cu.

The metals described above have long been used in the electronics industry. Some groups began to look at alloys such as constantan (55%Cu, 45%Ni) [83] or Manganin (84.2% Cu, 12.1% Mn, 3.7%Ni) [84, 85] because they are copper-rich alloys with structures that allow copper atoms to diffuse through them relatively easily. Panigrahi et al. [83] reported the use of a 2 nm constantan film in copper bonding at 150 °C that showed a 200 MPa shear strength and a resistance of 2×10^{-8} Ω-cm^2, essentially the same as with Manganin. The same group reported the use of a 3 nm film of Manganin in copper bonding at 140 °C with a pressure of 0.5 MPa [84], which gave a shear strength of 190 MPa and an electrical resistance of 1.1×10^{-7} Ω-cm^2. The Manganin film can slowly oxidize but does not oxidize in a noticeable way when left at room temperature in the atmosphere for a week [85].

Hong et al. [86] recently reported a detailed bonding mechanism with a metal passivation layer, in this case Pd. The contact of two bonding surfaces is first made by applying external stress. In this stage, voids are formed at the bonding interface. Then, diffusion of Cu atoms through the grain boundary of the passivation layer occurs with increasing bonding temperature, and amorphous Cu between passivation layers is formed, filling the voids. Postannealing after TCB induces recrystallization of amorphous Cu and polycrystalline Cu at the bonding interface, further enhancing the bonding quality and strength. Each stage of the mechanism was investigated using HR-TEM images and EDS analysis. Through this mechanism, they suggested that the bonding

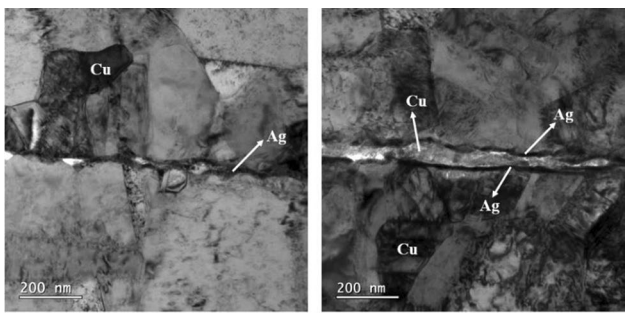


Fig. 7 Annealing effect in Cu bonding using an Ag nanolayer. **a** Bonded at 180 °C without annealing. **b** Bonded at 180 °C with annealing at 200 °C

temperature can be lowered with grain boundary diffusion of Cu atoms compared to conventional Cu–Cu direct bonding, which introduces lattice diffusion of high-crystallinity Cu.

2.2.4 Using Cu Insertion

Insertion bonding is a method in which a Cu pillar on one side of the bond is inserted into a concave receiver on the other side. The concave receiver is plated with Cu and is wider at the opening than it is at the bottom. Yang et al. [87] studied Cu pillar–concave structures with and without a polymer layer and reported that Cu pillar–concave structures with a polymer layer have several advantages, such as a simplified concave fabrication process, polymer stress release layers and reduced bonding time. Detailed structures of the Cu pillar and concave are shown in Fig. 8. The bonding was performed at 200 °C with a bonding force of 389 MPa per bump for 10 min in a regular atmosphere, and good bonding quality was obtained. In this method, the bonding temperature is sufficiently low, but the bonding pressure can be too high for CMOS device fabrication.

3 Cu Hybrid Bonding

Although numerous efforts have been made to facilitate direct Cu-to-Cu bonding or TCB, as discussed above, TCB still has some limitations in proliferating 3D HI. First, TCB is expected to be hardly scalable down to under a 10–15 µm pitch and requires a highly controlled environment during the whole bonding process to prevent surface oxidation [88]. Moreover, a high bonding temperature is needed to ensure sufficient interdiffusion of Cu. The relatively high temperature generates a thermal gradient in the bonding system and consequently results in degradation of the alignment and overlay accuracy [14]. The demand for high pressure also makes widespread implementation of TCB difficult, and it is even worse for large dies or wafers [89]. In this regard, hybrid bonding can be a paradigm shift in bonding technology and a potential solution to overcome these limitations and further extend bonding technology. Hybrid bonding refers to the simultaneous bonding of copper pads and surrounding dielectrics such as SiO_2, SiCN, and SiN. The general process of hybrid bonding is shown in Fig. 9. In hybrid bonding, widely studied for wafer-to-wafer bonding, dielectrics are actively used as a main bonding material, and Cu pads are first bonded at a relatively low temperature and then strengthened through thermal expansion of Cu by an additional annealing process. Dielectric inorganic materials are bonded well at low temperature and even at room temperature without external pressure when surfaces are appropriately treated. At low temperatures, thermally induced problems such as the generation of a thermal gradient can be alleviated. Moreover, the absence of bonding pressure makes integrating large dies easier and gives flexibility in architecture design, as hybrid bonding utilizes internal pressure generated by the difference in the coefficient of thermal expansion (CTE) between copper and the dielectric [14].

The strongest advantage of hybrid bonding is that the minimum pitch size of copper pads can be scaled down to 1 µm or even submicrons [90, 91]. A reduced pitch size enables improved accommodation of interconnections in a

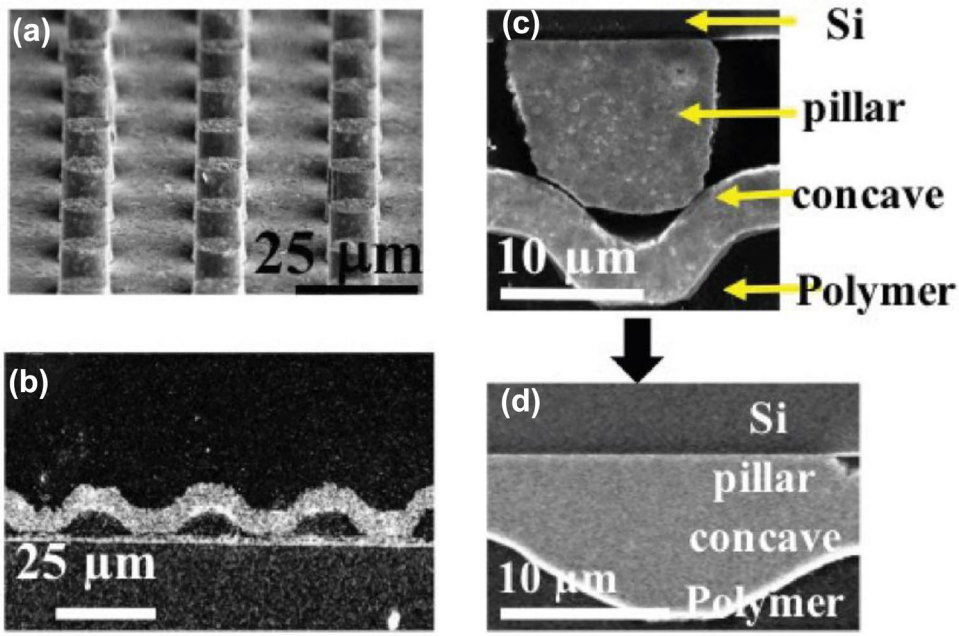


Fig. 8 SEM images of **a** Cu pillars and **b** Cu concaves. Cross-sectional images of a Cu pillar and concave **c** during bonding and **d** after bonding [87]

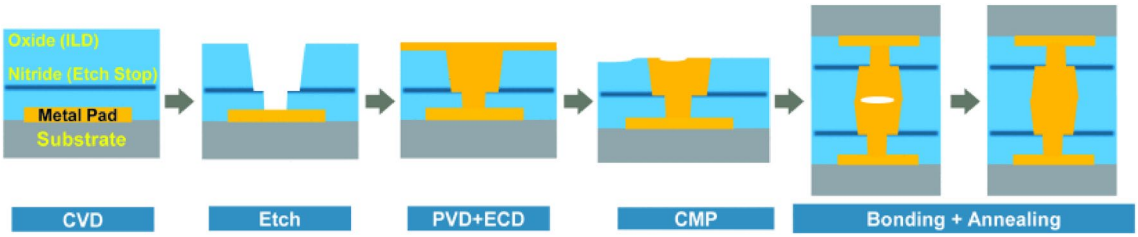


Fig. 9 Schematic diagram of the hybrid bonding process flow [90]

smaller area, leading to ultrahigh I/O density and achievement of higher computing power and higher bandwidth, which are essential to AI, 5G wireless communication and high-performance computing (HPC) [92–94]. Remarkably lower power consumption and lower latency can also be realized by the shrinkage of the pitch size with shortened electrical paths [1, 2, 88, 95]. Additionally, a reduction in the thermal resistance can be attained, improving the performance because there is no need to use polymer adhesives or underfill materials in hybrid bonding since dielectrics themselves automatically act as underfills [1].

The key process in hybrid bonding is the Cu CMP process, which controls surface planarization and determines Cu dishing [16, 96–98]. Additionally, erosion of the dielectric must be considered for fine-pitch pads since bonding occurs at the same time across the whole wafer [99]. Bonding between dielectrics should also be considered since dielectrics constitute most of the bonding area and virtually determine the bonding strength [16]. In addition, the prediction of the expansion volume of the copper pad, elimination of defects or particles, plasma treatment conditions and postbonding annealing should be considered to accurately accomplish hybrid bonding [1, 96, 97]. Not only are academic efforts being made to investigate hybrid bonding, but many semiconductor-related companies and institutes, such as Xperi, Samsung, IBM, IMEC and SK hynix, are now paying attention to hybrid bonding and developing high-tech solutions for hybrid bonding. In the following sections, recent developments in hybrid bonding will be discussed.

3.1 Cu/Oxide Hybrid Bonding

3.1.1 Direct Bond Interconnect (DBI) Technology

The most common and widely studied dielectric material for hybrid bonding is SiO_2 [100]. The well-known method of Cu/SiO_2 bonding is Xperi's Direct Bond Interconnect (DBI) [28, 31, 101–103], which is the most suitable copper bonding technology for CMOS fabrication. DBI technology is a form of copper dishing technology that has been commercially developed by Ziptronix [30] and is currently owned by Xperi [27, 30, 101–103]. DBI is a low-temperature hybrid bonding process that forms a SiO_2-to-SiO_2 bond at room temperature and a Cu-to-Cu bond at an appropriately elevated temperature [30]. The overall mechanism of DBI hybrid bonding, shown in Fig. 10, is as follows: The copper pads are lowered by approximately a few nanometers compared to the surrounding dielectric by controlling the Cu dishing in the Cu CMP process. After the CMP process, the wafer is cleaned by rinsing it in deionized (DI) water following surface activation and termination by plasma, conducted to prevent any chemical reaction of the exposed copper [102, 103]. Then, the two surfaces are carefully aligned and pressed together. Annealing heat is applied that strengthens the oxide bonds and causes the copper to try to expand above the surrounding oxide. The lower copper pad is forced into compression against the upper copper pad, and diffusion bonding results between them. This bonding occurs at the same time across the whole wafer, and thus, the Cu dishing uniformity of the wafer is critical. The successful

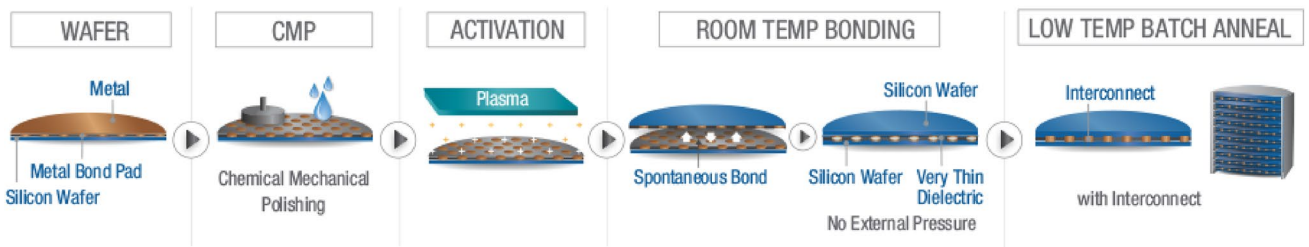


Fig. 10 Process flow of DBI technology [104]

bonding interface obtained using DBI technology is shown in Fig. 11a, presented by Xperi in 2009.

3.1.2 Effect of Cu Dishing and Dielectric Hydration

In the Cu/SiO_2 hybrid bonding system, SiO_2 is first bonded to another SiO_2, and then, Cu is bonded in the subsequent heat treatment process, during which thermal expansion is induced in Cu pads and bonding proceeds due to the occurrence of compressive stress at the copper/copper interface. Since CMP is the most crucial process to successfully bond dies or wafers, a variety of studies have been conducted to investigate the effect of the CMP process [16, 30, 105–107]. Fujino et al. [30] reported 300 mm wafer-level hybrid bonding with SiO_2 and 1×1 μm^2 Cu pads with a 2 µm pitch, during which the importance of CMP dishing and alignment was emphasized. Wafers were activated by nitrogen plasma and cleaned with 'megasonic' water before being bonded in vacuum, and then annealing was performed at 200 °C for seven hours. This study showed a good bonding interface without large voids except for voids at the edge of the bonding pad due to the galvanic corrosion effects between the Cu pad and barrier metal caused by the CMP process. Fraunhofer [105] discussed the effect of Cu dishing on hybrid bonding of a 4 µm Cu pad with a 10 µm pitch. They obtained an 80% contact area with 4 nm Cu dishing and postannealing at 250 °C using an oxygen or oxygen/hydrogen plasma to activate the oxide surface. In addition, Ji et al. [106] reported that the area of Cu bonding generally decreases with increasing dishing and with a lower annealing temperature. Beilliard et al. [108] discussed the effect of annealing conditions and the copper plastic response on Cu/SiO_2 hybrid bonding.

In contrast, Sony [107] proposed slight protrusion of Cu pads to enhance electrical connectivity rather than conventional dishing, suggesting that Cu dishing might work detrimentally, as the thermal expansion of Cu pads with an ultrafine pitch is less than a few nanometers even after the postbonding annealing process. They reported that the thermal expansion of a 1 µm pitch Cu pad with a pad size of 500 nm is only approximately 4 nm or less, meaning that it might be insufficient to entirely fill the gap between Cu dishing pads. Therefore, by using protruded Cu pads, hybrid bonding with high electrical yield was obtained at a 1 µm pitch level for face-to-face bonding and a 1.4 µm pitch level for face-to-back bonding. Cross-sectional SEM images of the bonding interface with an ultrafine pitch are presented in Fig. 11b.

Additional hydration treatment was studied to further lower the bonding temperature and reinforce the bonding strength. The hydration process with DI rinsing after surface activation by plasma treatment creates hydrophilic dielectric surfaces containing hydroxyl groups (–OH), and then, the surfaces are carefully aligned and pressed together at room temperature [1, 16]. The activated dielectrics on both surfaces with hydroxyl groups are bonded together at room temperature through van der Waals forces as well as hydrogen bonding, and the bonding is later strengthened by heating to an elevated temperature, with a transition to oxygen covalent bonds [109, 110]. After forming strong bonds between dielectrics, similar to the DBI process, each copper pad of the two substrates is forced into compression and starts to expand until it firmly forms contact with the other corresponding pad through interdiffusion, establishing an electrical connection during the annealing process. Samsung [16] reported hybrid bonding using hydrated dielectrics with different deposition conditions, showing a 38.9% increase in the adhesion strength.

3.1.3 Engineering the Microstructure of Cu

Similar to the works mentioned in 2.1, several studies on hybrid bonding have also attempted to improve the bonding nature of Cu pads by controlling the microstructure of Cu. Xperi and Lam [89] investigated the influence of the microstructure of Cu by engineering the electroplating process. As shown in Fig. 12, these corporations compared three different microstructures of Cu pads: standard BEOL Cu, nanotwinned Cu and fine-grained Cu. Both < 111 > -oriented nanotwinned Cu and fine-grained Cu showed better

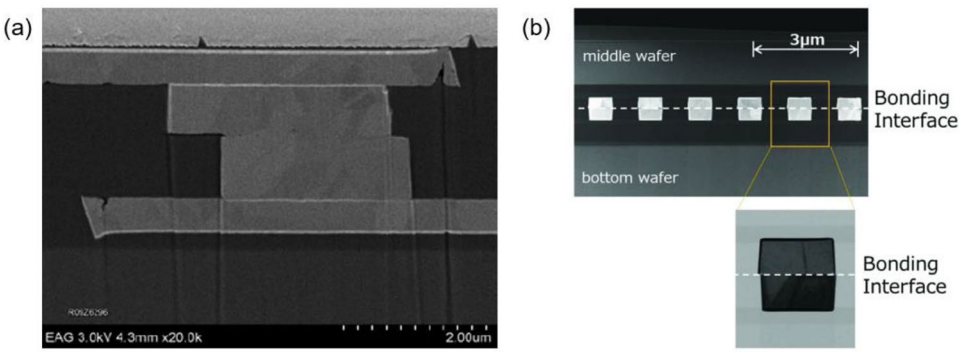


Fig. 11 Cross-sectional SEM images of the bonding interfaces obtained using **a** DBI [102] and **b** recent ultrafine pitch hybrid bonding [107]

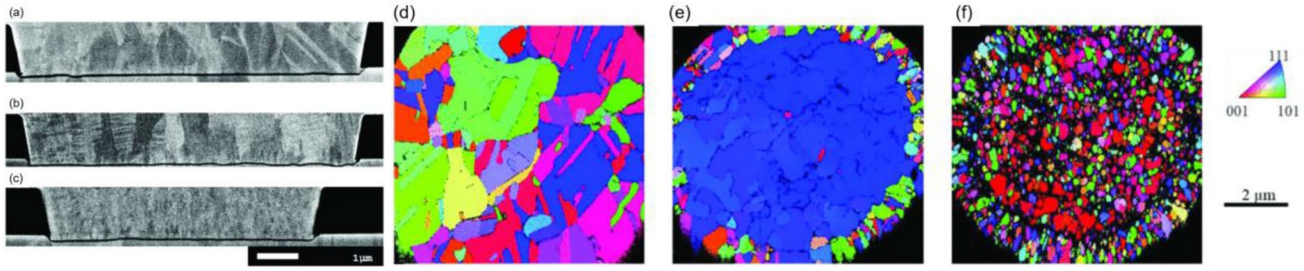


Fig. 12 Cross-sectional SEM images of **a** standard copper, **b** nanotwinned copper, and **c** fine-grained copper and EBSD images of **d** standard copper, **e** nanotwinned copper, and **f** fine-grained copper [89]

performance due to the fast diffusivity in the < 111 > direction and grain boundary self-diffusion, which has a lower activation energy for diffusion, respectively. The final annealing temperature to form strong metallurgical bonds was lowered by approximately 30 degrees, implying that a reduction in the thermal budget would be possible with microstructural engineering of Cu. Meanwhile, Chiu et al. [17] successfully realized hybrid bonding with nanocrystalline Cu. Low-temperature bonding occurred with 1 nm Cu dishing because the many grain boundaries existing in nanocrystalline Cu offered a fast diffusion path for Cu atoms. A pair of wafers were bonded at room temperature under a pressure of 1.06 MPa and postannealed at 150 °C for 1 h. The resulting bonding energy was 11.94 J/m^2 on average. In contrast, M. Murugesan et al. [15] discussed the enlargement of Cu grains with modified electroplating chemistry. Increased grain sizes in modified electroplating compared to conventional electroplating were confirmed with SEM images and inverse pole figure (IPF) images, which are shown in Fig. 13. Cu pads with oriented grains with sizes of 10–20 μm were bonded at room temperature and showed lower electrical resistance of Cu joints.

3.1.4 Cu/SiCN Structure

Recently, research on dielectric materials other than SiO_2 has also been performed. SiCN is thought of as a potential dielectric for hybrid bonding due to the lowest binding energy of the Si–C bond when a dangling bond is formed by plasma treatment and thus the superior bonding energy to SiO_2 [100, 111]. IMEC suggested [111] low-temperature SiCN-to-SiCN dielectric bonding with novel Cu/SiCN CMP processes. Excellent electrical and yield results were obtained across 300 mm wafers with a pitch size of 1.44 μm. This organization also showed the feasibility of a smaller pitch size of 0.72 μm and demonstrated the bonding approach with Cu

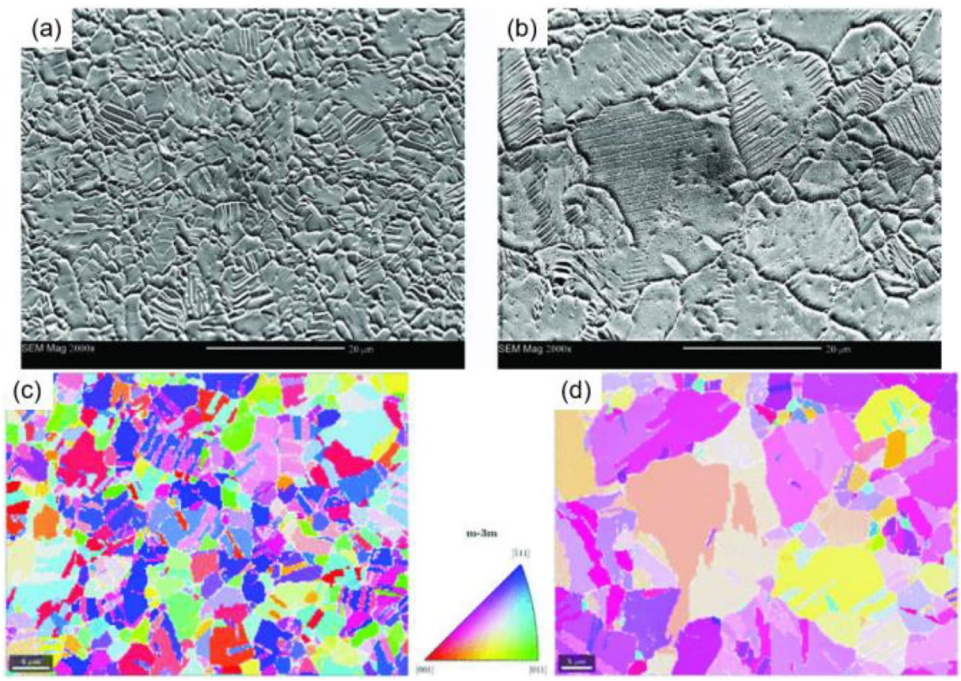


Fig. 13 Comparison of planar SEM images for **a** conventional electroplating and **b** modified electroplating and IPF images for **c** conventional electroplating and **d** modified electroplating [15]

pads of unequal size and different surface topographies. This organization also [3] reported deposition and densification of SiCN at temperatures below 200 °C. SiCN withstood the 350 °C annealing process, and the bonding interface showed a high bonding strength with no voids. They [112] further proposed the asymmetric design of Cu pad topography. The top device had a slightly protruded surface profile with a small pad size, and the bottom device had slightly recessed topography with a larger pad size. By designing different nanopad structures, they achieved a superior electrical connection of Cu/SiCN hybrid bonding at a 1.08 μm pitch with a compatible bonding Aligmnet tool tolerance limitation. IBM [113] also conducted Cu/SiCN hybrid bonding using plasma activation at room temperature. They revealed that voids at the bonding interface did not necessarily indicate good bonding by C-mode scanning acoustic microscopy (CSAM), although void-free bonding was necessary. Surface energy characterization by a single beam cantilever (SBC) was conducted, and the results showed that SiCN–SiCN bonding was relatively more stable and had a higher surface energy at approximately 2.0–2.5 J/m^2 than tetraethyl orthosilicate (TEOS)–TEOS bonding. Plasma-activated Cu/SiCN hybrid bonding at a pitch size of 6 μm showed a wider distribution than blanket SiCN-SiCN bonding, and thus, optimization of CMP dishing, pad shape and cleaning of the bonding interface should be established to eliminate weak bonding modes. Hynix [100] further studied the effect of plasma treatment and the composition dependence of the bonding strength in Cu/SiCN hybrid bonding. This company found that a high carbon ratio and O_2 plasma resulted in the best bonding strength among the studied conditions due to the largest number of silanol groups, which were made through breakage of the Si–C bond and subsequent DI rinsing. The CMP process can also affect the bonding performance of the Cu/SiCN system. The same group [96] observed that erosion of SiCN degraded the robust connection at the bonding interface because of interface voids resulting from the CMP process in the higher density region of Cu pads, whereas there were no voids in the lower density region. By controlling the RPM and pressure during CMP, this group realized void-free hybrid bonding under the condition of 5 nm Cu dishing with excellent electrical connectivity and produced the same yields as an existing DRAM product.

3.1.5 Novel Approaches

A few groups researched novel methods to achieve hybrid bonding. Q. Kang et al. [114] suggested a cohydroxylated Cu/SiO_2 hybrid bonding method, which is similar to the combination of plasma treatment in Sect. 2.2.1 and non-plasma treatment in Sect. 2.2.2. It is also similar to the dielectric hydration method in Sect. 3.1.2 except that they hydroxylated Cu pads as well. They made both Cu and SiO_2 surfaces have an –OH active layer by processing formic acid solution immersion and Ar/O_2 plasma activation. They optimized the surface activating process to establish a hydrophilic surface for both Cu–Cu and SiO_2–SiO_2 surfaces. During formic acid treatment, the proportion of hydrophilic CuO/$Cu(OH)_2$ increased up to a certain maximum point. Following plasma activation, organics were decomposed, converting CuO into $Cu(OH)_2$. Likewise, the surface of SiO_2 can be activated by formic acid treatment. Then, stable Si–O–Si bonds broke, and Si–OH bonds were generated by Ar/O_2 plasma activation. Cu/SiO_2 hybrid bonding in this study was achieved at 200 °C under a bonding pressure of 2.5 MPa for 30 min.

The same group [115] also proposed a co-hydrophilic strategy to facilitate Cu/SiO_2 hybrid bonding at low temperature. They used the combination of Ar/O_2 plasma and alkaline NH_4OH immersion to form hydrophilic functional groups on hybrid surfaces. During Ar/O_2 plasma activation, unstable Cu_2O converted into CuO and following the NH_4OH immersion process transformed CuO into -OH and -NH_2 groups with the oxidation and dissolution effects. For SiO_2 surface, Ar/O_2 plasma could break Si–O–Si covalent bonds to provide sites for the adsorption of functional groups and the NH_4OH solution provided abundant -OH and -NH2 groups for the sites. They confirmed the co-hydrophilization for Cu/SiO_2 hybrid surfaces using the combination of Ar/O_2 and NH_4OH with wettability characterization. Water contact angle of Cu and SiO_2 was decreased from 67.2° and 62.1° to 19.6° and 2°, respectively. Bonding was achieved at 200 C and a bonding pressure of 5 MPa for 30 min under atmosphere conditions and the bonding interfaces were void-less and homogeneous without any accumulation of oxides and nitrides. The maximum bonding strength of Cu–Cu surfaces was 21.4 MPa.

Li et al. [25] reported Cu-to-Cu bonding using selective thermal atomic layer deposition (ALD) of Co, which is similar to the metal passivation in TCB described in Sect. 2.2.3. The copper studs to be bonded are placed in position with a small gap between them. A Co solution or gas is circulated between the studs, and a layer of Co is selectively deposited between the Cu studs until the gap is filled. Connections between two 30 μm pads over a gap of 200 nm have been reported. The use of a metal passivation layer for Cu/SiO_2 hybrid bonding is difficult because a metal passivation layer has to be deposited only on the Cu surface and not on the oxide surface. However, this selective-area deposition method can be applied to Cu/SiO_2 hybrid bonding to deposit a metal passivation layer only on the Cu surface.

CEA-LETI and Intel [94] have put effort into developing a capillary self-assembly process as a promising technology for hybrid bonding. Two surfaces are prepared with pretreatment prior to bonding to obtain a hydrophilic surface, and then, a water droplet is dispensed on one side of the surface,

as depicted in Fig. 14. Afterward, hybrid bonding is realized as the dispensed liquid droplet generates a capillary force at the bonding interface, by which the two substrates can self-align. The droplet at the bonding interface is then evaporated, and the following annealing process turns weak bonds into covalent bonds. By altering the bonding surface of Cu/SiO_2 to a hydrophilic surface with appropriate treatments, they showed drastically increased alignment performance induced by the capillary force and potential throughput improvement.

3.2 Cu/Polymer Hybrid Bonding

Other alternative dielectric materials are polymers such as polyimide (PI), SU-8, or BCB. Polymeric insulation layers should be spin-coatable and thermally stable against diffusion of Cu in addition to having sufficient toughness to endure the CMP process [97]. They face several challenges, such as a low thermal budget, outgassing during curing and material height differences that occur during bonding, and are not suitable for fine pitches of a few μm or less, especially submicron pitches. Nevertheless, some studies have evaluated Cu/polymer hybrid bonding for low-temperature bonding, thick bumps (few to tens of μm), and void-free gaps between bumps. T. Shirasaka et al. [97] reported Cu/PI hybrid bonding, suggesting that PI is an appropriate candidate for polymeric insulators. PI was spin-coated, and a Cu protrusion was made after CMP and acid treatment. Cu/PI bonding, shown in Fig. 15, was achieved at 250 °C for 20 min under a pressure of 5 MPa and showed good electrical connection. Shie et al. [116] used nanotwinned Cu with PI as a dielectric material and compared it to Cu/nonconductive paste (NCP) hybrid bonding. In this case, the CMP process produced Cu dishing, and Cu and PI were bonded together at 200 °C for 30 min. Lu et al. [32] reported CuSn/PI hybrid bonding at 250 °C using asymmetric Cu/Ni/Sn-to-Cu/Ni bonding. They used Ni to prevent Cu oxidation and Sn to lower the bonding temperature. After the reliability test, they showed specific contact resistances at a level of 10^{-7} Ω-cm^2. Asymmetric hybrid bonding was also conducted by M. Weng et al. [4] using Au passivation and thermoplastic SU-8 polymer. Cu pads with Au passivation were patterned by a lift-off process, and the structures of each substrate were $Au/Cu/Su\text{-}8/SiO_2$ and $Au/Su\text{-}8/SiO_2$, which were bonded at the blanket wafer level at 200 °C for 5 min under a 10,000 N applied force. Hsiao et al. [33] performed Cu/BCB hybrid bonding at 250 °C and reported a shear strength of 40 MPa. When a polymer is used as a dielectric in hybrid bonding,

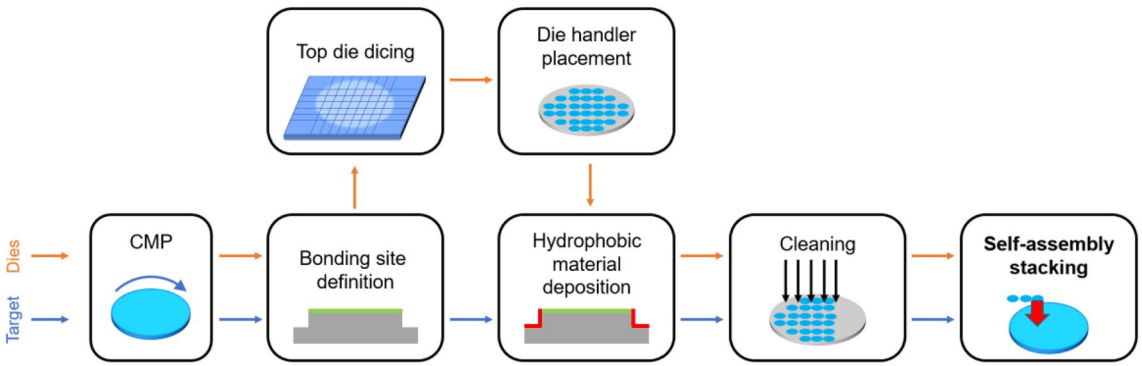


Fig. 14 Schematic process flow using the capillary self-assembly process proposed by CEA-LETI (reproduced from [94])

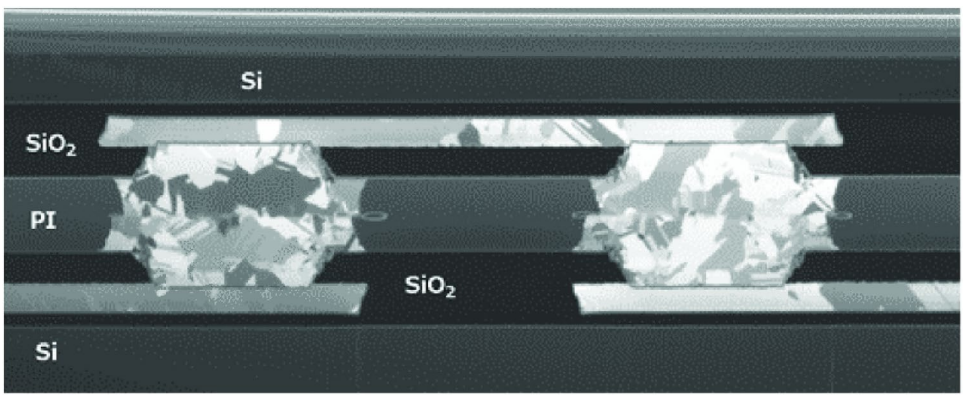


Fig. 15 Cross-sectional SEM image of a daisy-chain bonding interface with a Cu/PI system [97]

Cu bumps are generally formed first, and the polymer is then coated on. Hsiao et al. also spin-coated BCB after forming Cu bumps and then performed fly cutting with a diamond bit to obtain a flat and smooth bonding interface. Instead of fly cutting, Chidambaram et al. [34] used a polymer CMP process to flatten a polymer surface after coating and curing. Table 1 summarizes the TCB and hybrid bonding methods discussed in this paper. A manufacturing standard guide to hybrid bond strength or bond energy is not currently known precisely. However, based on the reliability of the BEOL interconnect, it is considered suitable if the bonding energy of the Cu–Cu bonding is 5 J/m^2 or more and the bonding energy of the oxide-oxide bonding part is 2 J/m^2 or more.

4 Perspectives and challenges

4.1 Perspectives

Hybrid bonding was initially developed for wafer-to-wafer (W2W) bonding in 3D packaging. Hybrid bonding technology is well developed at the wafer level because it is relatively easy to commercialize since the whole process of hybrid bonding can be performed in a vacuum cluster system after CMP [117, 118]. In 2016, Sony [119] commercialized wafer-level hybrid bonding for the first time in a CMOS image sensor (CIS), improving the performance by stacking memory with image-sensor logic [89, 120]. In 2020, multifunctional integration of DRAM and logic devices was presented by TSMC [121]. This company stacked 12 layers of DRAM using system on integrated circuit (SoIC) technology and achieved robust and reliable electrical characteristics. Currently, HBM (high bandwidth memory), a multilayer structure of DRAM, is bonded with microbumps, but as the number of I/Os increases to a pitch of 5 μm or less, hybrid bonding is needed. In the case of NAND, much research on bonding memory and logic using hybrid bonding has been conducted, and mass production is expected soon. Since the hybrid bonding method varies depending on the product, pad pitch and size, dielectric material, etc., it should be developed customized for the product.

W2W bonding is generally restricted to homogeneous integration or relatively low power systems such as high-density memory devices or CISs [16, 88]. To attain authentic 3D IC HI, various components such as memory, logic, AP, or graphics chiplets must be integrated at the die level. The design of the architecture should be flexible so that any requirements of a customer or a user can be met. These ultimate goals have recently drawn attention to die-to-wafer (D2W) or die-to-die (D2D) hybrid bonding for various system-in-package (SiP) structures. Figure 16 illustrates the different bonding requirements between the D2W and W2W bonding cases.

D2W hybrid bonding is expected to have much more versatility than W2W, as a large number of heterogeneous stacks can be integrated even with a decreased total thickness of the packaging. D2W hybrid bonding can fulfill the demands for many applications with advanced performance, high interconnection density, increased speed and power efficiency, wider bandwidth and better thermal management [3, 16]. The production yield would also be improved with a known good die (KDG) [97]. Xperi [122] showed a 4-die stacked structure with a pitch of 10 μm bonded at 200 °C using their D2W DBI Ultra technology. They also demonstrated die-level hybrid bonding with 2 μm Cu pads with a 4 μm pitch and showed that the electrical conductivity using a daisy chain structure was adequate as long as 80% of the area of the 2 μm pads was in contact [101]. AMD [2] presented the 3D V-Cache Ryzen 5000-series in 2021 and the Ryzen 7000-series in 2022, in which an SRAM die and a logic die are stacked using TSMC SoIC hybrid bonding. A cross-sectional SEM image of the 4-high stacked die and a schematic picture of the AMD 3D V-Cache are shown in Fig. 17. Integration of dissimilar chips and high connectivity will become major trends in semiconductor packaging technology in the future, and for this purpose, D2W hybrid bonding is expected to become a key technology.

4.2 Challenges

There are many challenges to overcome to facilitate the mass production of D2W hybrid bonding because it has stricter conditions and is more sensitive, as even small changes in process conditions can result in a very large change in bonding outcomes [16, 94, 123]. First, unlike W2W hybrid bonding, D2D or D2W hybrid bonding has an unexpected difficulty in maintaining clean and flat surfaces due to the detritus produced by the die singulation process [14, 78, 92, 97, 98, 105]. Hybrid bonding is highly surface-sensitive, so careful control of surface contamination and flatness is extremely important. Otherwise, defects, including debris, burrs, and any particulates created during dicing, especially near the die edges, would induce the bonding surface to form an uneven topography [98]. Voids are eventually easily generated from these defects, leading to bonding results that have poor electrical connectivity or even open-circuit failure since an only nanometer-sized particle can result in a micron-sized void [124]. Fraunhofer IZM [105] reported a study on particle contaminants caused by dicing. This institute compared the conventional dicing process with dicing using a protective layer and stealth dicing and addressed the need for defect-free dicing and handling procedures for good bonding.

The bonding surface topography is also affected by the CMP process. Cu dishing must be controlled at the level of tens of angstroms considering the expansion volume

Table 1 Summary of bonding methods reviewed in this paper

No.	Bonding type	Category	Method	Bonding temperature (°C)	Bonding pressure (MPa) (or bonding force)	Bonding shear strength (MPa) (or bonding energy)	References
1	Direct Cu-to-Cu bonding	2.1	Using a stress difference	100	0.25	120	Panigrahi et al. [45]
2			Using (111)-oriented nanotwinned Cu	300	90	N/A	Shie et al. [37]
3		2.2.1	Forming gas plasma treatment	300	0.42	5.55 J/m^2	Kim et al. [49]
4			Argon plasma treatment	250	10	43.1–61.2	Chiang et al. [50]
5			Ar/N2 mixed plasma treatment	RT	N/A	20.3	Tan et al. [54]
6			Ar/N2 sequential plasma treatment	260	0.9	62	Park et al. [56]
7		2.2.2	Wet chemical treatment	400	25 kN	4.1–7.9 J/m^2	Park et al. [57]
8			Formic acid vapor treatment	240	250	150	Jangam et al. [35]
9			Xenon flash laser method	250	10	31	Liang et al. [60]
10		2.2.3	Self-assembled monolayer method	250	0.25	> 60	Tan et al. [62]
11			Using conductive adhesive epoxy with Ni particles	150	0.3 N	N/A	Ma et al. [65]
12			Cu nanoparticles	250	1.08	25.36	Li et al. [66]
13			Cu nanoparticles	250	10	32.4	Mou et al. [67]
14			Cu nanoparticles	250	8	20	Zuo et al. [68]
15			Ag nanoparticles	180	50	> 9	Liu et al. [70]
16			Citrate coated Ag nanoparticles	260	1	~ 27.5	Wang et al. [72] and Zhang et al. [73]
17			Ti layer	175	0.25	190	Panigrahi et al. [74, 76]
18			Ti layer	200	30	30	Park et al. [75]
19			Au layer	140	0.3	> 200	Bonam et al. [77]
20			Pd layer	150	1.91	N/A	Huang et al. [78]
21			Pt layer	200	N/A	8.2	Liu et al. [79]
22			Ag layer	180	30	14	Kim et al. [80]
23			Ag layer	180	90	N/A	Chou et al. [81]
24			Constantan layer	150	0.4	200	Panigrahi et al. [83]
25			Manganin layer	140	0.5	190	Panigrahi et al. [84]
26		2.2.4	Using a pillar-concave structure	200	389	N/A	Yang et al. [87]

Table 1 (continued)

No.	Bonding type	Category	Method	Bonding temperature (°C)	Bonding pressure (MPa) (or bonding force)	Bonding shear strength (MPa) (or bonding energy)	References
27	Cu hybrid bonding	3.1.1	Direct Bond Interconnect (DBI) method	RT	0	N/A	Enquist et al. [102]
28		3.1.2	Using convex Cu pads	RT	0.01	N/A	Fujino et al. [30]
29			Hydration treatment	RT	N/A	0.7–2.5 J/m^2	Kim et al. [16]
30		3.1.3	Using (111)-oriented nanotwinned Cu and fine-grained Cu	RT	0	N/A	Mirkarimi et al. [89]
31			Using nanocrystalline Cu	RT	1.06	11.94 J/m^2	Chiu et al. 17]
32			Using enlargement of Cu grains	RT	N/A	10.6–12.5	Murugesan et al. [15]
33		3.1.4	Cu/SiCN hybrid bonding	RT	N/A	> 2 J/m^2	Beyne et al. [111]
34			Cu/SiCN hybrid bonding	RT	N/A	N/A	Kim et al. [112]
35			Cu/SiCN hybrid bonding	RT	N/A	> 2 J/m^2	Sakuma et al. [113]
36		3.1.5	Hydroxylating Cu pads using formic acid solution immersion and Ar/O_2 plasma activation	200	2.5	N/A	Kang et al. [114]
37			Surface co-hydrophilization using Ar/O_2 plasma and NH_4OH immersion	200	5	21.4	Kang et al. [115]
38			Using selective deposition of Co	200	0	N/A	Li et al. [25]
39			Using a capillary self-assembly process	RT	N/A	N/A	Bond et al. [94]
40		3.2	Cu/PI hybrid bonding	250	5	> 20	Shirasaka et al. [97]
41			Nanotwinned Cu/PI hybrid bonding	200	2.8	N/A	Shie et al. [116]
42			CuSn/polymer hybrid bonding	250	1.23	~ 6.5	Lu et al. [32]
43			Cu/SU-8 polymer wafer-level hybrid bonding using Au passivation	200	10 kN	1449 N	Weng et al. [4]
44			Cu/BCB hybrid bonding	250	20 kN	40	Hsiao et al. [33]

of Cu, and the local surface roughness must be retained below 1 nm to ensure strong dielectric-to-dielectric bonding [16, 88]. The bonding pattern density, pattern configuration, and topography from the underlying layers are other factors that might have an impact on the bonding surface topography and thus should also be carefully determined [88]. Hence, ultraclean and extremely smooth surfaces of both Cu and the dielectric should be viable along with handling and attachment of prepared dies.

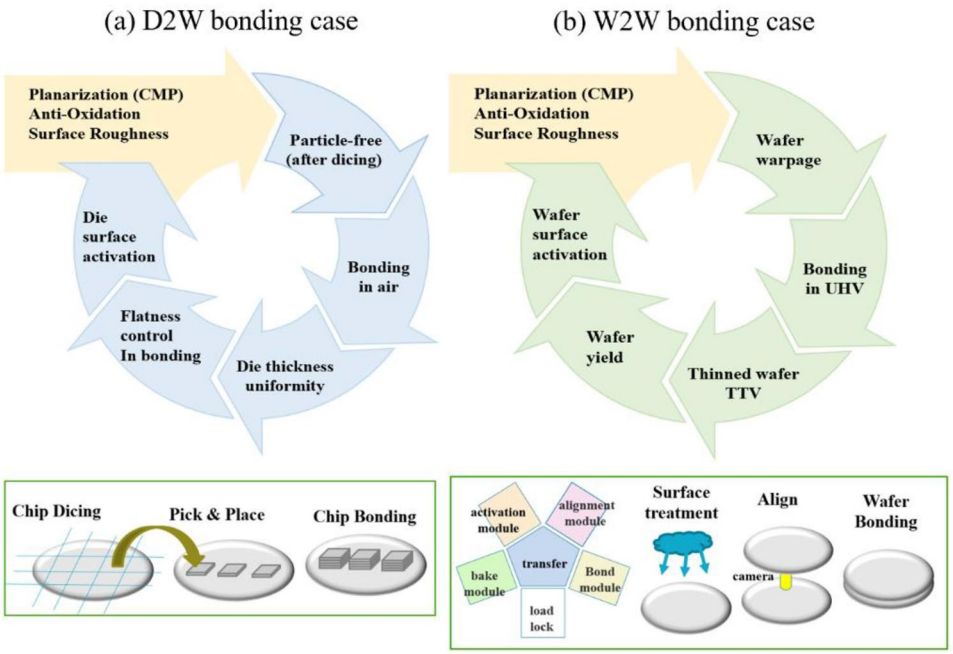


Fig. 16 Comparison of D2W bonding and W2W bonding requirements

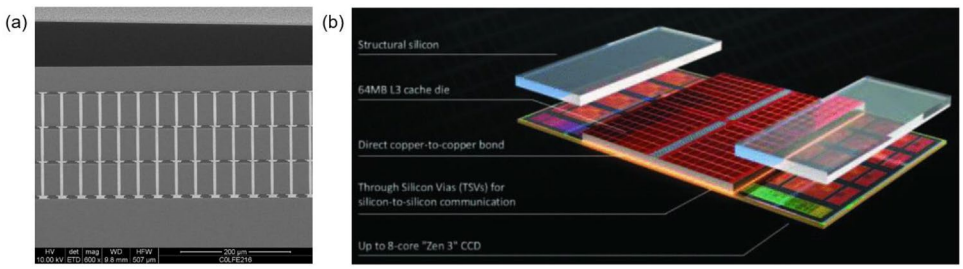


Fig. 17 **a** Cross-sectional SEM image of a 4-high stacked die demonstrated by Xperi [122]. **b** Schematic view of the AMD 3D V-Cache stacked die [2]

Furthermore, lowering the thermal budget of hybrid bonding is another major obstacle to conquer for the purpose of high bonding yield. The entire process of D2W hybrid bonding must proceed at temperatures as low as possible. Otherwise, stacked various integrated chips, such as memory and/or logic devices, would fail to function properly regardless of how excellent the bonding strength is. On account of the high demand for low-temperature bonding [125], room temperature hybrid bonding methods [15–17, 30, 89, 94, 102, 111] have recently been suggested. However, most of them include postbonding annealing processes. The annealing temperature and time in the postbonding process should also be minimized to lower the entire thermal budget of bonding technology. Moreover, postbonding annealing can change several detailed conditions of the bonding structure, including the dishing level, and cause several reliability issues, even though the initial pad design and the amount of protrusion are thoroughly adjusted [16, 123]. Precise alignment with submicron accuracy, different bonding structures in the case of double-sided bonding, and increased keep-out zones, which are unused die areas, are other considerations for successful bonding and high yields [98].

Finally, a variety of reliability issues must be considered [13, 90, 126]. According to the heterogeneous integration roadmap (HIR) [127], the tightest pitch in hybrid bonding would be the submicron scale to satisfy the increasing need for high-density interconnects. Pitch shrinking of bonding pads results in an increase in current density, and the increased current density is likely to cause electromigration (EM), which is one of the serious reliability risks for BEOL interconnects to date [17], as well as for Cu bonding pads. Applied Materials [90] studied the EM risk in a hybrid bonding structure with a SiN capping layer on SiO_2. The current density at the edge of the bonding joint is predicted to increase by a few orders of magnitude and consequently increase the temperature due to Joule heating. The atomic concentration decreased to 30% of the initial concentration at the exit of the current and increased to 120% at the entrance of the current, which means that migration of Cu atoms occurred due to the current flow. Dielectric reliability issues, such as copper diffusion and dielectric breakdown,

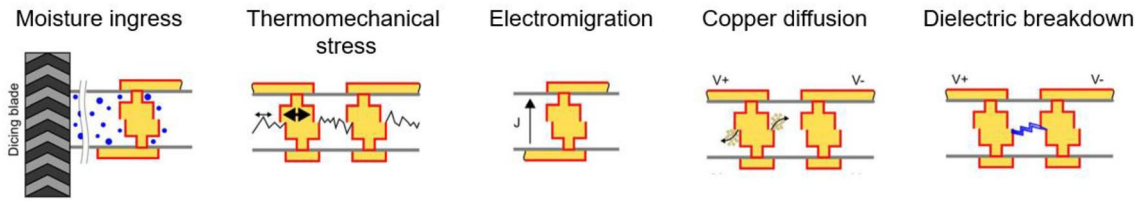


Fig. 18 Possible reliability issues in hybrid bonding (reproduced from [126], © The Electrochemical Society. Reproduced with permission from IOP Publishing. All rights reserved)

should also be considered since dielectric spacing is reduced along with the shrinkage of bonding pads. It is widely known that the drift of Cu in the dielectric is accelerated by a larger applied bias voltage and smaller spacing of the dielectric. Increasing the electric field usually increases the rates of dissolution, transport, and dendrite growth of metallic ions in electrochemical migration (ECM) [128]. A similar effect is also applied for the migration of Cu ions through the dielectric, leading to a higher risk of short circuit failure. TSMC [129] also suggested that misalignment or overlay of bonding pads might deteriorate dielectric reliability by providing a shorter conduction path or breakdown path. For both EM and TDDB reliability risk, barrier materials might have to be applied to relieve the concentrated current density and suppress the formation of voids or hillocks as well as prevent dielectric breakdown resulting from the diffusion of Cu. Potential reliability issues, including moisture ingress, thermomechanical stress, EM, copper diffusion and dielectric breakdown, are described in Fig. 18 [126].

5 Conclusions

This paper reviews various studies on TCB and Cu/dielectric hybrid bonding with the importance of copper bonding technology in next generation 3D HI. Copper oxide removal, additional oxidation prevention, and enhanced diffusion of Cu atoms are key requirements for complete copper bonding. In particular, hybrid bonding has recently become very important for fine-pitch and high-density interconnections. Therefore, a full understanding of the hybrid bonding mechanism and fabrication process for mass production is necessary. The optimization of Cu bonding to ensure electrical and mechanical reliability must also be continuously developed. Cu bonding technology implemented with HI is expected to be a solution that bridges the gap between device and system packaging.

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Declarations

Conflict of interest The authors declare no conflict of interest.

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