IMAGE LICENSED BY INGRAM PUBLISHING

A Review on Hybrid Bonding Interconnection and Its Characterization

WITH CONSIDERING THE performance computing growing exponentially, heterogeneous integration becomes as a solution for combining more logic, memory, and specialty chiplets in each area to accelerate computing. Hybrid bonding interconnection (HBI) is one of the most important technologies to heterogeneous integration, which is defined as a bonding along with a "hybrid" interface (metal-metal and dielectric-dielectric). It enables a connection from a silicon chip to another with direct metal pad to pad connection. The technology increases the density of the contact and shorten the interconnect distance between components. In

Digital Object Identifier 10.1109/MNANO.2024.3358714
Date of current version: 19 April 2024

CHIEN-KANG HSIUNG AND KUAN-NENG CHEN

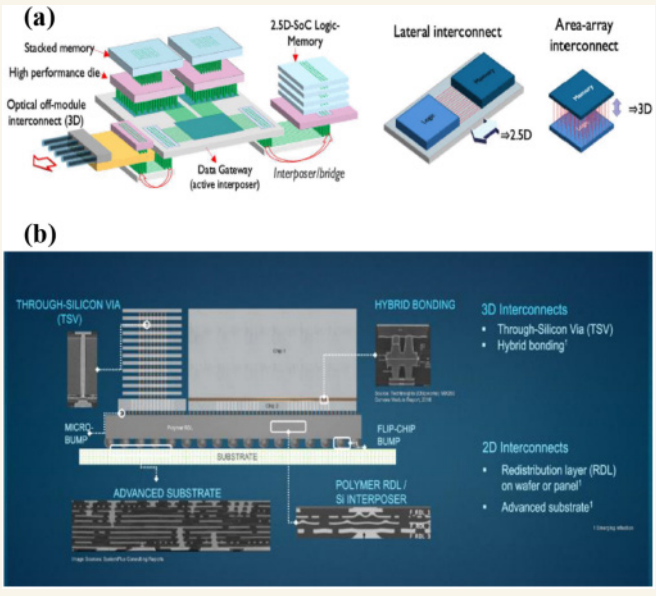


FIGURE 1 (a) A high-performance computing system integrated by 2.5D (interposer to connect local high bandwidth memories and optical transceiver modules) and 3D (stacked memory and stacked performance die) integrations [10], and (b) key interconnection structures of 2.5D and 3D integrations [42].

this paper, we review the modern technologies of Hybrid bonding interconnection with characterization of the contact interfaces of metal to metal and dielectric to dielectric. Also, we raise a novel method to perform a low cost, organic dielectric based, low process temperature hybrid bonding interconnection for wider packaging application needs.

HETEROGENEOUS INTEGRATION ENABLED BY ADVANCED CONNECTION

Advanced packaging techniques have arisen as a crucial driver pushing the continuous evolution and downsizing of electronic devices. In the realm of performance, power, area-cost, and time-to-market (PPACt) [1], the focus has shifted onto 3D integrated circuit (3DIC) technology, drawing considerable attention. The modern explanation of "3D" extends beyond the confines of the backend package process, embracing heterogeneous integration within the silicon chip integration as well. This review delivers a comprehensive overview on advanced package interconnection technologies, with a dedicated emphasis on the scope of hybrid bonding interconnection technology for 3DIC fabrication.

Numerous methodologies exist for establishing interconnections within packages. Traditional copper micro-bumps, created through the fabrication of copper pillars with lead-free solder caps, have been adopted as the interconnect paradigm for mid-to-high-end flip-chip packages. Ponte Vecchio architecture presented by Intel is a leading-edge example which utilize micro-bumps to assemble the 3D stacked chipset system [2]. The micro-bumps with fine pitches support designs with 30-40 μm pitches by employing bump diameters of 20-25 μm and elevations ranging from 10-20 μm for interconnection spacing [3]. The advanced micro-bumps for silicon chip to chip connection can be further scaled down in pitch [4], published by tsmc for specific mobile, IoT and client applications. The interconnection process based on copper micro-bumps is following mature procedures to fabricate electroplated bumps with specified metals followed by mass reflow process, and finally succeeded by precisely controlled thermal compression bonding (TCB) techniques at assembly [5]. Micro-bump interconnection can be applied for leading edge flip-chip package and package-on-package (PoP) type of packaging structures. Very fine pitch micro-bump (pitch down to 18-25 μm) can be applied for silicon chip to chip interconnection, as a cost-effective way for consuming products.

However, scaling of package interconnections continues pushing the cutting-edge package technology development. In recent times, the application of silicon chip integration has garnered significant attention, allowing diverse functional silicon components, to combine into an integrated silicon assembly, known as chiplet integration [6]. The term "chiplet" represents the smaller size integrated circuit (IC) with specific functionality. Multiple chiplets can be assembled by advanced interconnection technologies. In the case, a unique technology, hybrid bonding interconnection, is developed for the needs of finer pitches and lower latency comparing with conventional copper micro-bumps. Hybrid bonding interconnection enables a connection from a silicon chip to another with direct metal pad to pad connection, where the "hybrid" means the bonding interface includes metal-metal and dielectric-dielectric. The connection pad pitch can be further reduced from that was made by micro-bumps.

The hybrid bonding interconnection method has the potential to increase the data throughput between chiplets. Differ from a monolithic chip, a chiplet assembles chips based on their specific functions. This concept essentially based on a functional partitioning of the system on chip (SoC). The partitioned silicon chips, characterized by distinct I/O protocols, can be interconnected using frontend packaging processes. Anticipated developments point towards to enabling partitioning at levels within the monolithic chip, manifesting as 3D "System on Chip" (3D-SoC) partitioning. Figure 1 shows a high-performance computing system with 2.5D (interposer to connect local high bandwidth memories and optical transceiver modules) and 3D (stacked memory and stacked performance die) integrations and their key interconnection structures [7].

This approach facilitates the creation of multiple distinct functional chips, manufactured on separate source wafers, which

are subsequently assembled into individual chips using appropriate packaging techniques. Refer to the segmentation from tsmc, these techniques can be categorized into Backend 3D platform and Frontend 3D platform, as Figure 2 shows [8].

Backend 3D platform is geared towards connections between silicon and packaging components (for example, interposer or substrate) or between package modules (for example, fanout modules). For this purpose, well-established interconnection technologies such as silicon interposers (2.5D) and Fanout are employed.

Frontend 3D platform, on the other hand, concentrates on silicon process integration achieved by stacking chips together with applying hybrid bonding interconnection. This IC stacking can be accomplished using various connection technologies, including chip to wafer [9], [10], chip to chip [11], and wafer to wafer [12], [13] stacking methods. Frontend 3D technology facilitates the assembly of multiple functional silicon chiplets while carefully considering factors such as interconnection bandwidth for data transfer, power delivery, mechanical robustness, and thermal management. Typically, a key requirement for chip stacking involves scaling down the contact pad pitch to sub 10 µm or even less than 1 µm [14], [15]. The scaling of Frontend 3D chip stacking is closely correlated to the development of hybrid bonding interconnection. Collaborating with feature structures like through silicon vias (TSV), through oxide vias (TOV), and inter-die gap fill (IDGF), these interconnection links vertically stack chips of the same or differing sizes. In forthcoming sections of this article, we will elucidate the functions of these structures and outline the integrated process flow of packaging. In Table 1 [41], we summarize the connection technologies described above, their dimension, and relative performance.

ENABLEMENT OF CHIPLET INTEGRATION

The chiplet integration approach presents several advantages. Firstly, it benefits from the assembly of known good dies (KGD) [16]. Since chiplets amalgamate individual functional chips, KGD can be pre-sorted for assembly. Secondly, each individual chip can be manufactured using its optimal process node during semiconductor production. The overall chiplet manufacturing process is not restricted by the most advanced functional blocks; different processes can be employed for chiplets. Thirdly, the footprint of each functional chip can be more flexibly adjusted compared to a monolithic chip design. With these advantages in mind, hybrid bonding interconnection technology empowers semiconductor companies to realize heterogeneous integrated (HI) chiplets spanning various functions, technology nodes, and sizes. This technology enables the combination to function as a unified product. The ultimate application of hybrid bonding interconnection assembled chiplets is aimed at domains such as high-performance computing and artificial intelligence, both of which are experiencing exponential growth, even as traditional 2D transistor scaling faces limitations and increased costs.

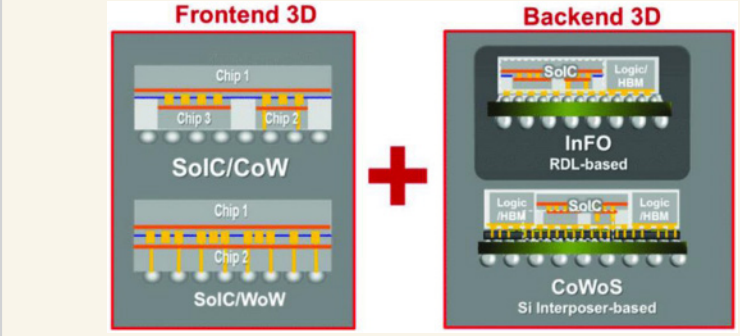
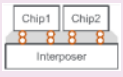
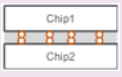
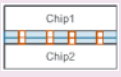
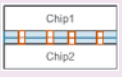


FIGURE 2 Frontend 3D and Backend 3D heterogeneous brief and their integration. Frontend 3D includes system on integrated chip (SoIC) with chip on wafer (CoW) and wafer on wafer (WoW) technologies. Backend 3D includes integrated fanout (InFO) and CoWoS (chip on wafer on substrate) technologies. Frontend 3D and Backend 3D can collaborate for the advantages on PPACt come from system level integration [8].

TABLE 1 Advanced Connection Technologies [41].

TECHNOLOGY	BUMP	MICRO-BUMP	HBI	HBI
Applications	2.5D Interposer	3D Chip Stacking	3D Chip Stacking	3D Chip Stacking
Sample				
Interconnect	Solder	Solder	Cu-Cu	Cu-Cu
Connection Pitch	~36um	~25um	<10um	<3um
Connection Density	0.06X	0.13X	1X	9X
Performance (1/Delay)	0.05X	0.035X	1X	<0.79X
Bandwidth Density	0.003X	0.0455X	1X	7.11X
Energy/bit	458X	20X	1X	0.75X

HYBRID BONDING INTERCONNECTION MANUFACTURING APPROACH

Hybrid bonding interconnection enables a connection from a silicon chip to another with direct metal pad to pad connection. The hybrid bonding interconnection considers both Cu-Cu bonding and dielectric-dielectric bonded interfaces, requiring detailed process controls with handling copper and dielectric materials, which can be performed by thermal compression bonding (TCB) and direct bonding interconnection (DB or DBI).

Thermal compression bonding (TCB) technology has found extensive application in advanced flip-chip solder bonding processes [17], [18]. This versatile technology can also be adapted for hybrid bonding interconnection with a broader process window, especially regarding surface conditions. Nevertheless, traditional TCB involves longer heating time for the handling chucks.

An alternative bonding technique known as direct bonding intercon-

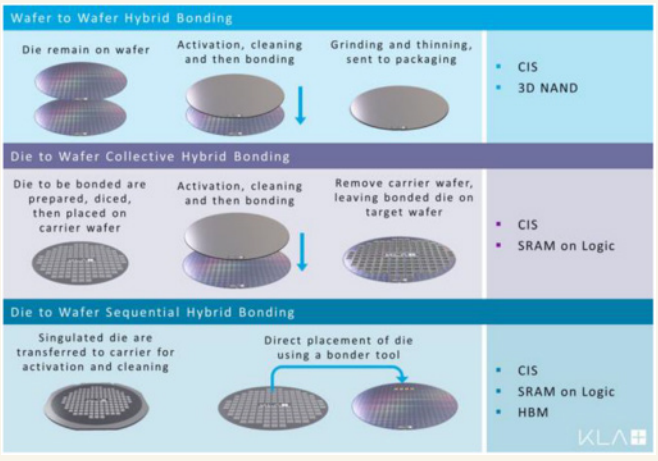


FIGURE 3 Different hybrid bonding interconnection fabricated by bonding methods. Wafer to wafer (WtW) bonding and die to wafer (DtW) bonding are two primary procedures, and die to wafer collective bonding is a combined procedure of a reconstituted wafer to wafer bonding [21].

nection (DB or DBI) [17] has been implemented in production cases. This method involves placing the die directly onto the bottom wafer after surface activation treatment at room temperature or a low heating temperature. This approach significantly reduces concerns about coefficient of thermal expansion (CTE) mismatch during die placement. A subsequent post-annealing step is necessary to complete the hybrid bonding interconnection interface bonding, and the bonding mechanism will be explored in upcoming sections of this article. The DB method offers potential enhancements in throughput, overlay accuracy, and overall cost of ownership. However, maintaining high surface cleanliness, dielectric surface conditions, and effective control of copper dishing are vital for achieving successful bonding yields.

In some advanced demonstrations, the DB method has showcased remarkable precision, achieving wafer-to-wafer overlay within less than 300 nm (3 sigma within wafer, WIW) [19], and even as low as 100 nm under optimized conditions. These outcomes illustrate the method's capability to handle hybrid bonding interconnection bonding with sub-micron contact pad sizes. In the case of conventional fabrication of a hybrid bonding interconnection involving polycrystalline copper pads (Cu-Cu connection) and SiO2 dielectric (SiO2-SiO2 bonding), a post-annealing process with 280 – 400 °C is necessary to address concerns related to contact resistance and grain growth at the bonded interface. However, such high-temperature annealing poses challenges for thermally sensitive devices, such as DRAM. Therefore, there is an interest in developing low-temperature processes for hybrid bonding interconnection formation, typically below 220 °C. This research area aims to expand the range of applications for advanced heterogeneous integration.

HYBRID BONDING INTERCONNECTION SCHEME

Hybrid bonding interconnection can be accomplished through various bonding procedures, people also consider wafer-to-wafer (WtW) bonding, chip-to-chip (CtC) bonding, or chip-to-wafer (CtW) bonding methods. WtW bonding has found successful applications in high-volume production of image sensors [20], developed by SONY with Ziptronix (Xperi) Direct Bonding Interconnection (DBI) technology [21]. Notably, there has also been recent reporting on the integration of logic chips with passive wafers [22]. CtC bonding, on the other hand, is significantly tailored to the realm of 3D stacked DRAM applications, and the development of low temperature hybrid bonding interconnection (LT-HBI) techniques has become a focal point for this application [23]. CtW bonding finds its use in assembling logic chips to SRAM and logic-to-logic integration. Ongoing research is encompassing a wide array of areas, such as advanced integration involving more stacked components and solutions aimed at cost reduction [24].

The comparison of different hybrid bonding interconnection procedures is outlined in Figure 3 [25]. The two primary bonding methods for stacking silicon chips or IC package modules are wafer-to-wafer (WtW) bonding and die-to-wafer (DtW) bonding. An innovative approach known as "collective bonding" technology combines the reconstitution procedure of die-to-wafer (DtW) with a subsequent WtW bonding process.

DtW finds widespread application in hybrid bonding interconnection for both heterogeneous and homogeneous integration scenarios. The process is accomplished with the dicing of the functional device wafer, followed by the transfer of known good dies (KGD) onto a temporary carrier, typically in a frame form (with a temporary adhesive tape) carrier. The frame-form carrier undergoes surface activation and cleaning steps, after which the KGDs are positioned onto a functional wafer. The advantages of the DtW procedure include: (1) the preliminary sorting of KGDs before bonding, (2) the flexibility to accommodate various die sizes, and (3) the capability to work with different wafer types, resulting in fewer mismatch impacts. However, one limitation of this technology is the consideration for throughput. Enhancing bonding speed, ensuring high die-to-wafer accuracy, and achieving cost-effectiveness remain the central objectives in the development of DtW technology.

At the forefront of innovation, a fully integrated DB CtW bonding tool concept has emerged. This integrated tool encompasses multiple clusters interconnected within a mainframe. The key modules, including the surface activation (plasma treatment) module (designed to accommodate frame-type carriers), cleaning module, and DB bonding module, are closely linked to minimize the queue time between surface activation and DB bonding. This configuration also ensures superior particle control

compared to handling individual tools. The integrated DB CtW bonding tool brings substantial benefits to complex heterogeneous chiplet integration, contact pad scaling down, and low-temperature hybrid bonding interconnection integration scenarios.

WtW bonding technology has seen extensive development over time, tracing its roots back to dielectric Fusion Bonding involving the contact of dielectric layers deposited on the surfaces of silicon wafers. This method has been applied in various contexts such as the production of backside illuminated CMOS image sensors (BSI-CIS), MEMS devices, and backside power distribution networks (BSPDN). The extension of fusion bonding to enable hybrid bonding interconnection with embedded metal and dielectric defines as WtW bonding. Similar to DtW, WtW bonding can be handled by thermal compression fusion bonding and DB modes (contacting at room temperature followed by post-annealing).

WtW hybrid bonding interconnection introduces additional considerations compared to fusion bonding. Achieving precision chemical-mechanical polishing (CMP) processes is vital for managing total thickness variation (TTV) and uniformity of copper pad surface profiles. In 12-inch WtW bonding cases, nano to sub-nano scale dielectric surface roughness (Ra) is a necessary condition, alongside precise control of nano-scale copper surface dishing profiles. Controlling wafer warpage is critical for ensuring yield and overlay alignment during wafer-to-wafer contact, while the condition of bonded wafer edges affects the subsequent wafer thinning process, often necessitating edge trimming to maintain conformity without misalignment or edge bevel effects [26].

Integrated WtW bonding tool modules have been employed in mass production for years. These integrated tools encompass major modules such as preactivation plasma treatment, wafer cleaning, and bonding. Optionally, UV bond and alignment verification modules can be linked to the mainframe for sequential WtW bonding process integration. Conventional WtW direct bonding processes take place in atmospheric conditions, prioritizing throughput and cost of ownership (COO) considerations.

> The selection of hybrid bonding interconnection bonding dielectric and metal constitutes the most pivotal decision, contingent upon the type of silicon chiplets to be integrated. Regarding dielectric materials, silicon oxide fabricated through plasma enhanced chemical vapor deposition (PE-CVD) utilizing tetraethoxysilane (TEOS) precursor has found wide application in hybrid bonding interconnection contexts.

Comparing WtW bonding to DtW bonding, the former offers advantages in terms of throughput and a simpler process flow. However, one limitation of WtW bonding is that KGD cannot be individually bonded to other KGD at the bottom wafer. The loss in wafer yield depends not only on the bonding process itself but also on the yield of individual bonded wafers. A more recent development is the Collective Bonding technology [27], which introduces an additional step involving the transfer of KGD to create a reconstituted wafer ("ReCon" wafer), followed by the WtW bonding process. However, this technology requires further demonstration to establish its capabilities. In essence, the bonding overlay accuracy of the Collective Bonding method results from combining temporary DtW and permanent WtW bonding overlays. When compared to the DtW process, the collective bonding technology may not achieve the same level of fine-pitch hybrid bonding interconnection product handling.

HYBRID BONDING INTERCONNECTION INTERFACE CHARACTERIZATION

Figure 4 illustrates the process integration for hybrid bonding interconnection formation. The process can be broadly categorized into three major segments: Hybrid bonding pad formation, Alignment and Contact, and Post-Bond Process. This review paper will focus on using DtW hybrid bonding interconnection as an example to delve into the key performance indices of the major process modules.

Hybrid bonding pad formation is typically associated with the top metal layer of the backend of line (BEOL). Detailed distinctions between face-to-face, face-to-back, and back-to-back [28], [29] hybrid bonding pad formation are not covered in this paper. Instead, the focus is on characterizing the contact pad surface. The standard process, in alignment with BEOL procedures, involves dielectric deposition, dielectric via etching, barrier/seed layer deposition, electroplated via filling, followed by the removal of excess metal through

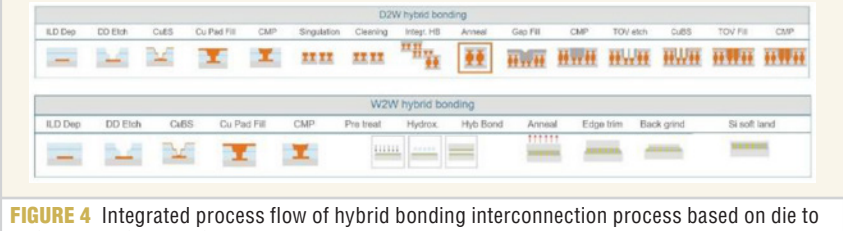


FIGURE 4 Integrated process flow of hybrid bonding interconnection process based on die to wafer and wafer to wafer integrations [42].

TABLE 2 Candidates for dielectric and metal options of hybrid bonding interconnection.

COPPER MICROSTRUCTURE	DEPOSITION TECHNOLOGY (*CONVENTIONAL METHOD)	GRAIN	POST BONDING ANNEAL	ADDITIONAL PROCESS DETAILS
Polycrystalline Copper	*Electroplating	Polycrystalline copper	>280°C	Industrial baseline Bonding interface grain growth is related to native oxidation
Nanotwinned Copper	*Electroplating Magnetron Sputtering	Twinned structure	200–250°C	Highly related to chemistry Higher hardness copper, CMP process is critical to bonding quality.
Fine Grain Copper	*Electroplating	Fine grain copper	200–250 °C	Highly related to chemistry Fine grain microstructure stability is sensitive to process temperature and queue time.
Passivation Metal (Interface Metal, IF)	*PVD Electroless Plating	Passivation metal on polycrystalline copper	180–250 °C	Multiple candidates on passivation metal selection. Additional cost from passivation metal fabrication.

CMP process. The final metal CMP step also contributes to refining the bonding metal contact surface.

The selection of hybrid bonding interconnection bonding dielectric and metal constitutes the most pivotal decision, contingent upon the type of silicon chiplets to be integrated. Regarding dielectric materials, silicon oxide fabricated through plasma enhanced chemical vapor deposition (PE-CVD) utilizing tetraethoxysilane (TEOS) precursor has found wide application in hybrid bonding interconnection contexts. Silane precursors are also under scrutiny due to their lower process temperatures. Given that the silicon oxide bonding mechanism hinges on covalent bond formation through siloxane links, the quality of the silicon oxide layer deposited on the chip or wafer side significantly influences defects at the bonding interface. In recent years, various dielectric materials have been investigated for specific hybrid bonding interconnection applications. SiCN is being considered for applications with low process thermal budgets, potentially enabling post-annealing at temperatures below 250 °C [30]. Aluminum nitride (AlN) is explored as a bonding dielectric interface material offering high thermal conductivity [31].

In terms of contact metal, electroplated copper remains the prevalent choice. To lower the annealing temperature for Cu-Cu bonding, several novel metal schemes have been proposed, including nanotwinned copper (ntCu) [32], fine-grain copper [33], and a passivation metal structure [34]. Table 2 compiles the candidates for dielectric and metal options in the context of hybrid bonding interconnection.

In the formation of Cu-Cu connections, the bonding surface should be slightly recessed compared to the surrounding dielectric surface prior to hybrid bonding. Additionally, stringent specifications are imposed on copper dishing tolerances achieved through the CMP process [35], [36]. The amount of copper dishing required is influenced by factors such as hybrid bonding contact pad dimensions (shape, diameter, and depth), bonding methods (DB or TCB), and annealing conditions. Achieving an ideal Cu-Cu bond less defect at bonding interface is depending on minimizing the organic impurity residue, high cleanliness of the hybrid bonding pad, limited oxidation, and well controlled copper protrusion behavior during annealing heating step. Inadequate dishing can lead to excessive copper protrusion at annealing temperatures, resulting in gaps between dielectric layers. Conversely, excessive dishing may give rise to voids caused by insufficient Cu-Cu connection.

Copper density presents a significant challenge in the CMP process. Elevated copper coverage can cause heightened erosion in areas with high copper density, potentially leading to delamination within those regions. Based on our experience, careful monitoring of localized erosion becomes imperative when copper density surpasses 20%.

State-of-the-art CMP processes offer exceptional dishing control across 12-inch wafers, achieving sub-nanometer total thickness variation (TTV) control (3 sigma). Tuning CMP conditions to optimize outcomes for various pitches and copper coverage scenarios stands as an ongoing objective for manufacturers. Combining endpoint detection with real-time profile control (RTPC) during the polishing process proves beneficial in improving TTV control during hybrid bonding pad formation.

HYBRID BONDING MECHANISM AND CHARACTERIZATION: DIELECTRIC BONDING

In the case of SiO_2 dielectric bonding, particularly within the context of the DB hybrid bonding interconnection method, the initial attachment is facilitated by Van der Waals forces generated through hydrogen bonding networking between oxygen and hydrogen atoms derived from absorbed wafer molecules at the bonding interface [37], [38]. The die-to-wafer attachment process occurs at low temperatures, typically below 100 °C, often at room temperature. This mechanism largely governs SiO_2-SiO_2 direct bonding by leveraging absorbed water layers, in which water molecules form a cluster at temperatures below 100 °C. Subsequent to this, a thermal process is employed to anneal the bonded structure. As the temperature rises above 100 °C, water is capable of diffusing around the bonding interface, leading to adhesion

through hydrogen bonding originating from silanol groups on the surface of SiO_2 dielectric layers. At temperatures around 200 °C, covalent bonds like siloxanes can form. Further elevation of temperature, nearing 700 °C, permits the SiO_2-SiO_2 interface to close nano-gaps at the interface. This mechanism, often referred to as SiO_2 viscous flow, occurs through annealing at high temperatures, as depicted in Figure 5. However, as mentioned previously, the annealing temperature is constrained by the functionality of the integrated circuits. Standard backend of line (BEOL) processes usually allow for process temperatures of 300-350 °C, which is commonly employed for logic device process integration. In contrast, DRAM devices are more sensitive to temperature, necessitating an annealing temperature of 220 °C or even lower to avoid detrimental effects on functionality.

In cases involving SiCN-to-SiCN dielectric bonding [30], a solution with low annealing temperatures is introduced for hybrid bonding interconnection. SiCN dielectrics offer the advantage of achieving a high bonding energy (>2 J/m^2) at low annealing temperatures (around 250 °C), as reported. SiCN-SiCN bonding showcases distinct interfacial properties. Some research indicates that the cross-section of SiCN-SiCN bonding presents an interface with approximately 10 nm of oxide-rich material, evident by the strong dark contrast observed in transmission electron microscopy (TEM) images. electron energy loss spectroscopy (EELS) studies suggest that the oxide-rich interface likely corresponds to SiO_2.

Activation treatments for dielectric surfaces, terminated by hydrophilic functional groups, are essential. The extent of dangling bonds is closely tied to activation conditions, followed by a step that involves water absorption, typically accomplished through a water wash or a queue time. Various concepts have been proposed for activation processes, such as wet processes employing a dilute HF (DHF) solution and dry processes like O_2 plasma, N_2 plasma, Ar plasma, or their combinations involving forming gas to achieve surface activation treatment [39].

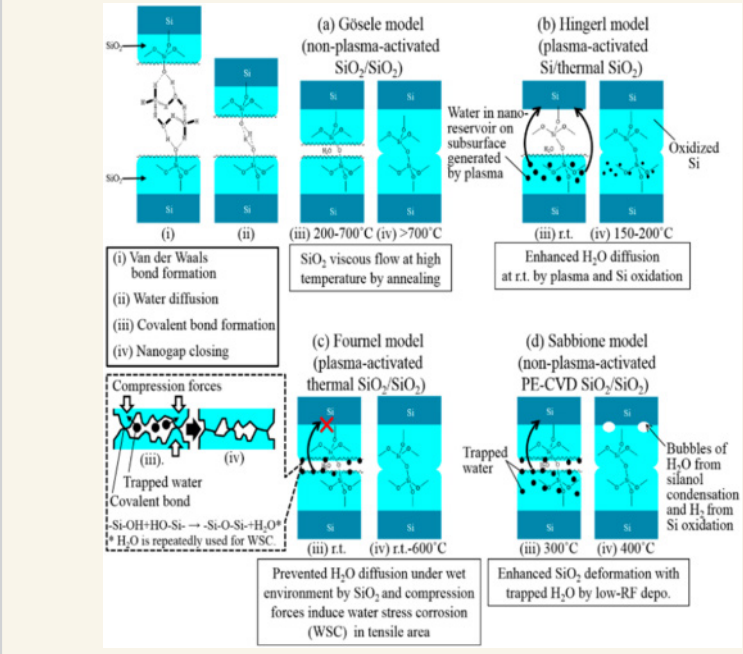


FIGURE 5 Interface reaction mechanism of SiO_2 – SiO_2 bonding based on fusion bonding process.

Dielectric bonding voids represent a significant defect that affects the reliability of the bonding interface, leading to an increase in non-ideal electrical property. To ensure dependable 3D stacking, it is crucial to achieve a void-free bonding interface. The occurrence of SiO_2-SiO_2 voids at the bonding interface has been linked to the temperature of post-bond annealing processes, with void formation primarily taking place at annealing temperatures above 350 °C in the presence of water. Additionally, dangling bonds are also thought to contribute to void formation during the direct bonding annealing process. However, SiCN-SiCN bonding interfaces tend to exhibit fewer voids, or even none, after post-bond annealing. Research indicates that void formation correlates with the density of dangling bonds. SiCN-SiCN interfaces show a higher density of dangling bonds, which can lead to chemical reactions between dangling bonds and water molecules.

Polymer dielectric materials are now being considered as potential candidates for hybrid bonding interconnection. Previous research has shown that benzocyclobutene (BCB) based polymers can be bonded at temperatures below 180 °C [43]. Furthermore, based on our recent study, photo-imageable polyimide (PI) has demonstrated reliable bonding capability at temperatures below 250 °C.

HYBRID BONDING MECHANISM AND CHARACTERIZATION: COPPER INTERCONNECTION

In achieving an ideal hybrid bonding interconnection, Cu-Cu connections are typically facilitated through grain boundary migration. This phenomenon occurs after thermal compression (in the case of TCB) or post-bonding annealing (in the case of direct bonding). The mechanism of Cu-Cu grain migration, so called grain growth in industrial, at a specific temperature and compression pressure can be modeled using a surface creep model. This model postulates that the pressure gradient acts as the driving force, compelling layers of atoms to migrate and fill the spacing of the bonding interface. Factors such as copper surface roughness, bonding time, temperature, and pressure play pivotal roles in the bonding formation process [40]. Cu-Cu grain migration (grain growth) can be monitored by cross-section TEM analysis, Figure 6(a) shows a general mapping of morphology-bonding strength correlated to bonding temperature [45].

To reduce the bonding temperature, surfaces with high copper diffusivity are

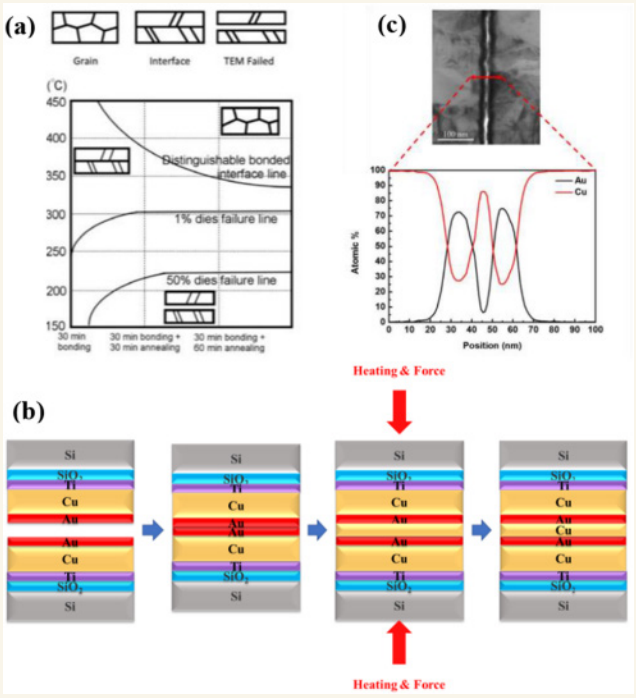


FIGURE 6 Schematic illustration of Cu-Cu bonding, (a) a general mapping of Cu-Cu interface morphology as an index of bonding connection quality [45], (b) with Au passivation layer and its bonding mechanism [44], (c) bonding interface analysis in the case of passivation metal method. A continuous copper can be inspected at the bonding interface as a result of Cu atom diffusion [34].

considered. Surfaces that are highly oriented toward Cu (111) exhibit enhanced surface diffusivity. Moreover, during low-temperature bonding (as low as 250 °C), the theoretical bonding time for (111) surface diffusion is notably shorter than that for grain boundary diffusion. However, it is essential to account for grain boundary formation when considering experimental bonding times for (111) surfaces. Thus, a precise control on (111) oriented Cu microstructure during the Cu pad manufacturing process remains a critical factor in enabling low-temperature bonding.

A method involving the application of a passivation metal on the copper surface to achieve low-temperature Cu-Cu bonding has been introduced [44]. Specific passivation metal, such as gold (Au) and others, can be applied to cover the copper pad surface, effectively preventing copper oxidation in the atmosphere. Subsequently, during the thermal processes involved in hybrid bonding interconnection, such as temperature cycling bonding (TCB) or post-direct bonding (DB) annealing, Cu atoms can diffuse through the passivation layer. In this process, the metal passivation layer enhances the diffusion of Cu atoms. The diffused Cu atoms form a continuous connection phase, enabling the entire bonding process to be conducted at a temperature as low as 120 °C. The passivation metal method is with high mass production potential since it can be fully integrated in packaging manufacturing process. Figure 6(b) shows a schematic metal stacking and interconnection formation mechanism, and Figure 6(c) shows a cross-section of the Cu-Cu bonding by passivation metal method.

In the case of direct bonding, since the annealing is performed without additional compression force, the key challenge is to achieve fully-bonded Cu-Cu metal interfaces/pads at low thermal budget such as 200–250 °C to mitigate adverse thermal impact to the device. To the case, the material coefficient of thermal expansion (CTE) is also the factor to optimize Cu-Cu bonding at lower annealing temperature. A modeling work pointed that with providing different microstructure of copper, it can provide up to 40% improvement in CTE. With capping metal on copper, CTE can be improved up to 43% at optimal capping layer thickness. The results show that CTE plays a significant role in bond quality and 40% improvement on CTE can facilitate the full Cu/Cu pad bonding at desired temperature regimes.

Finally, thermo-mechanical reliability in copper pads were analyzed for various temperature and CTE scenarios. Thermo-mechanical simulations clearly show that with the current dishing amount (10 nm), it is not possible to obtain good Cu-Cu bonding even at 300 °C with Cu CTE. Improved CTE from selective Cu alloy, improves the Cu-Cu bonding at 300 °C. At lower annealing temperature of 250 °C, the CTE increases similarly reduce the Cu-Cu gap and suggests a potential solution for success Cu-Cu bonding at lower thermal budget.

In achieving an ideal hybrid bonding interconnection, Cu-Cu connections are typically facilitated through grain boundary migration. This phenomenon occurs after thermal compression (in the case of TCB) or post-bonding annealing (in the case of Direct Bonding). The mechanism of Cu-Cu grain migration at a specific temperature and compression pressure can be modeled using a surface creep model. This model postulates that the pressure gradient acts as the driving force, compelling layers of atoms to migrate and fill the spacing of the bonding interface. Factors such as copper surface roughness, bonding time, temperature, and pressure play pivotal roles in the bonding formation process.

LOW COST POLYMER DIELECTRIC BASED LOW TEMPERATURE HYBRID BONDING INTERCONNECTION

A novel low-temperature hybrid bonding technology is presented to target the fabrication of a multi-layer redistributed line (RDL) structure. This technology is devised to create a low-layer-count and fine-pitch RDL structure via the semi-additive RDL process on separate glass carriers. These high-layer-count RDL layers are subsequently assembled using a low-temperature hybrid bonding process (<200 °C). The novel process flow is

named as "Hyper RDL". The utilization of low-temperature hybrid bonding for the RDL introduces a substantial reduction in accumulated stress during the process, thereby mitigating issues related to warpage. A reference process flow of Hyper RDL fabrication is shown in Figure 7(a). The low temperature hybrid bonding interconnection is applied with considering an interface with photosensitive polyimide (PSPI) dielectric bonding and passivation metal gold (Au) enhanced low-temperature Cu-Cu bonding. Based on previous investigation, passivation metal (Au) could establish low-temperature Cu-Cu bonding connections by thermal compression mode at 200 °C as well as polyimide to polyimide bonding. In the case, an additional post annealing process (250 °C/30 min) is optional. The process integration adopted in this reference process flow involves a Passivation Metal (Au)/Ti/Cu metal stacking scheme.

Remarkably, the study reveals that even low-modulus PSPI with a surface roughness (Ra) of 10 nm can be successfully bonded. Further enhancements to the PSPI-PSPI bonding interface are achieved through the implementation of pre-bonding surface activation processes. Figure 7(b) shows structured Hyper RDL fabricated by LTHBI with the cross-section inspections.

Overall, Hybrid RDL demonstrates the application of a novel hybrid bonding technology that enables the creation of multi-layer RDL structures at low temperatures. The applications of this process module can be broad, such as high density interconnection (HDI) substrate manufacture, high layer count RDL stacking in wafer level package, and RDL based packaging module integration in wafer form or in panel form. The results highlight the potential for reduced stress accumulation and improved bonding interfaces, showcasing the potential of this technology for advanced semiconductor packaging.

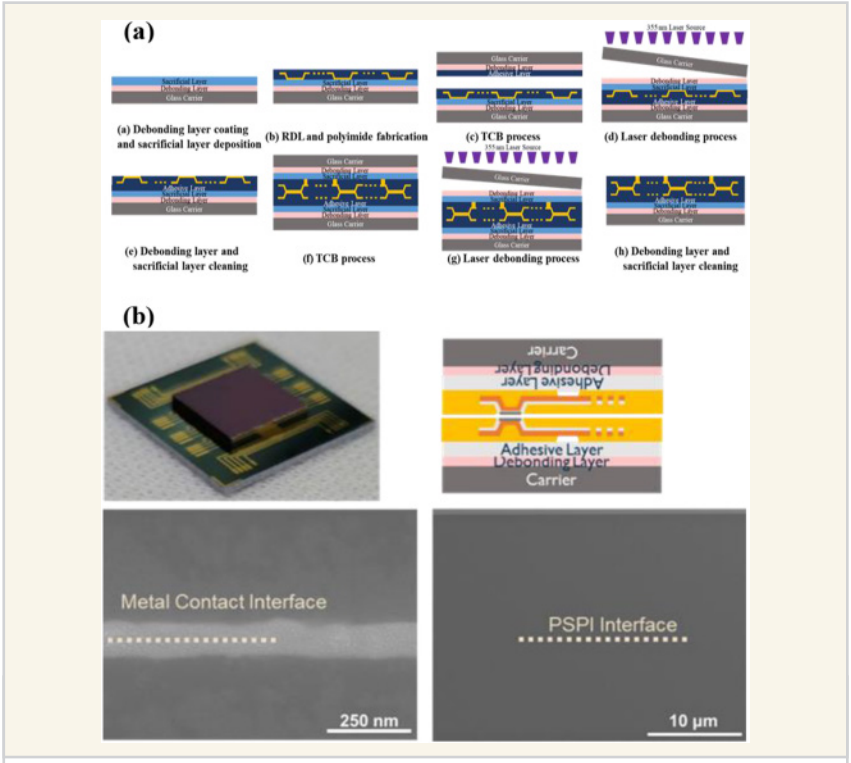


FIGURE 7 (a) The process flow of Hyper RDL; such process includes a hybrid bonding interconnection based on photosensitive polyimide (PSPI) dielectric and passivation metal (Au) covered on copper. (b) The structured Hyper RDL fabricated by LTHBI with the cross-section inspections.

CONCLUSION

In summary, this article delves into advanced packaging techniques, with a specific focus on 3D integrated circuit (3DIC) technology. The evolution of packaging methods, such as micro-bump interconnections and hybrid bonding, is explored in the context of improving performance and integration. The emergence of Chiplet technology, enabling the assembly of functional silicon components, is highlighted as a crucial development for heterogeneous integration.

The article outlines different bonding methods, including die to wafer (DtW), chip to chip (CtC), and wafer to wafer (WtW) bonding. Collective Bonding, combining DtW and WtW bonding, is also discussed. The importance of process integration and interface characterization in achieving successful hybrid bonding is emphasized.

Two primary bonding mechanisms are detailed: dielectric bonding and copper interconnections. Silicon oxide dielectric bonding is explained through hydrogen bonding and annealing processes. The role of different dielectric materials, such as SiCN and AlN, is explored. Conventional Cu-Cu interconnections involve copper grain boundary migration requiring high temperature. (111) Cu oriented surface contributes low-temperature bonding capability. Finally, a passivation metal method to achieve the lowest bonding temperature with reliable Cu-Cu interconnection interface is introduced.

The article concludes by introducing a novel low cost and low temperature hybrid bonding technology, Hyper RDL, based on redistributed line (RDL) structures. The benefits of low-temperature hybrid bonding, its benefit from stress reduction, advancements in passivation metal enhanced Cu-Cu bonding and photosensitive polyimide bonding are discussed.

Overall, the article underscores the significance of advanced packaging methods in the evolution of semiconductor devices, focusing on 3DIC technology and its potential to reshape the landscape of electronic systems.

ACKNOWLEDGMENTS

This work was supported in part by Semiconductor Research Corporation, the "Center for the advanced Semi-

conductor Technology Research" from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the Ministry of Education in Taiwan, in part by the National Science and Technology Council, Taiwan, T-Star center project "Future Semiconductor Technology Research Center", under Grants NSTC 113-2634-F-A49-008-, NSTC 112-2221-EA49- 163-MY3, and NSTC 110-2221-E-A49-086-MY3.

Parts of the perspectives and opinions presented in this paper were drawn from consultations with APDC of Applied Materials Inc. and Packaging Department of MediaTek Co. Ltd.

ABOUT THE AUTHORS

Chien-Kang Hsiung (khsiung.st09@nycu.edu.tw) is with the International Colleague of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu, 300, Taiwan.

Kuan-Neng Chen (corresponding author: (knchen@nycu.edu.tw)) is with the Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, 300, Taiwan.

REFERENCES

[1] S. Ramamurthy, "Applied materials advances heterogeneous chip integration with new technologies for hybrid bonding and through-silicon vias," in *Proc. Appl. Mater. Investor Meeting*, 2023, pp. 1–3. [Online]. Available: https://ir.appliedmaterials.com/node/26486/pdf

[2] W. Gomes et al., "Ponte Vecchio: A multi-tile 3D stacked processor for exascale computing," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 42–44.

[3] R. Agarwal et al., "3D packaging for heterogeneous integration," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf.*, 2022, pp. 1103–1107.

[4] *TSMC North America Technology Symposium*, Apr. 2023. [Online]. Available: https://pr.tsmc.com/english/news/3021

[5] M. H. Chan et al., "Comparison of 3D packages with 20um bump pitch using reflow soldering and thermal compression bonding," in *Proc. IEEE 71st Electron. Compon. Technol. Conf.*, 2021, pp. 481–486.

[6] S. R. Srinivasa et al., "Design methodology for scalable 2.5D/3D heterogenous tiled chiplet systems," in *Proc. IEEE 23rd Int. Symp. Qual. Electron. Des.*, 2022, pp. 1–4.

[7] E. Beyne, D. Milojevic, G. Van der Plas, and G. Beyer, "3D SoC integration, beyond 2.5D chiplets," in *Proc. IEEE Int. Electron Devices Meeting*, 2021, pp. 3.6.1–3.6.4.

[8] Y. H. Chen et al., "Ultra high density SoIC with sub-micron bond pitch," in *Proc. IEEE 70th Electron. Compon. Technol. Conf.*, 2020, pp. 576–581.

[9] W. Zhou et al., "Critical challenges with copper hybrid bonding for chip-to-wafer memory stacking," in *Proc. IEEE 73rd Electron. Compon. Technol. Conf.*, 2023, pp. 336–341.

[10] V. N. Sekhar, M. D. Kumar, P. Lianto, S. C. Chong, and V. S. Rao, "Cu damascene process on temporary bonded wafers for thin chip stacking using cu-cu hybrid bonding," in *Proc. IEEE 73rd Electron. Compon. Technol. Conf.*, 2023, pp. 564–570.

[11] H. Clauberg, A. Rezvani, V. Venkatesan, G. Frick, B. Chylak, and T. Strothmann, "Chip-to-chip and chip-to-wafer thermocompression flip chip bonding," in *Proc. IEEE 66th Electron. Compon. Technol. Conf.*, 2016, pp. 600–605.

[12] N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and thermal analysis of bumpless build cube 3d using wafer-on-wafer and chip-on-wafer for near memory computing," in *Proc. IEEE 73rd Electron. Compon. Technol. Conf.*, 2023, pp. 772–777.

[13] H. Moriceau et al., "Overview of recent direct wafer bonding advances and applications," *Adv. Natural Sci.: Nanosci. Nanotechnol.*, vol. 1, 2010, Art. no. 043004.

[14] E. Beyne, "The 3-D interconnect technology landscape," *IEEE Des. Test*, vol. 33, no. 3, pp. 8–20, Jun. 2016.

[15] A. A. Bajwa et al., "Heterogeneous integration at fine pitch (≤ 10 µm) using thermal compression bonding," in *Proc. IEEE 67th Electron. Compon. Technol. Conf.*, 2017, pp. 1276–1284.

[16] T. Fukushima et al., "Multichip self-assembly technology for advanced die-to-wafer 3-D integration to precisely align known good dies in batch processing," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 12, pp. 1873–1884, Dec. 2011.

[17] G. Gao et al., "Chip to wafer hybrid bonding with cu interconnect: High volume manufacturing process compatibility study," in *Proc. Int. Wafer Level Packag. Conf.*, 2019, pp. 1–9.

[18] H. Ren, Y.-T. Yang, and S. S. Iyer, "Recess effect study and process optimization of sub-10 µm pitch die-to-wafer hybrid bonding," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf.*, 2022, pp. 149–156.

[19] A. Jouve et al., "1µm pitch direct hybrid bonding with <300nm wafer-to-wafer overlay accuracy," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf.*, 2017, pp. 1–2.

[20] M. Goto et al., "Pixel-parallel three-layer stacked CMOS image sensors using double-sided hybrid bonding of SOI wafers," *IEEE Trans. Electron Devices*, vol. 70, no. 9, pp. 4705–4711, Sep. 2023.

[21] L. Wang et al., "Direct bond interconnect (DBI) for fine-pitch bonding in 3D and 2.5D integrated circuits," in *Proc. Pan Pacific Microelectron. Symp.*, 2017, pp. 1–6.

[22] S. Felix, S. Morton, S. Stacey, and J. Walsh, "29.4 wafer-level stacking of high-density capacitors to enhance the performance of a large multicore processor for machine learning applications," in *Proc. IEEE Int. Solid- State Circuits Conf.*, 2023, pp. 424–426.

[23] C. H. Tsai, T. Ku, M. F. Chen, W. C. Chiou, C. T. Wang, and D. Yu, "Low temperature SoIC™ bonding and stacking technology for 12/16-hi high bandwidth memory (HBM)," in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2.

[24] J. Wuu et al., "3D V-cache: The implementation of a hybrid-bonded 64MB stacked cache for a 7nm x86-64 CPU," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2022, pp. 428–429.

[25] S. Hiebert, "Hybrid bonding takes heterogeneous integration to the next level," 2023. [Online]. Available: https://www.3dincites.com/2023/05/hybrid-bonding-takes-heterogeneous-integration-to-the-next-level/

[26] S.-W. Kim et al., "Novel Cu/SiCN surface topography control for 1 µm pitch hybrid wafer-to-wafer bonding," in *Proc. IEEE 70th Electron. Compon. Technol. Conf.*, 2020, pp. 216–222.

[27] T. Uhrmann, J. Burggraf, and M. Eibelhuber, "Heterogeneous integration by collective die-to-wafer bonding," in *Proc. Int. Wafer Level Packag. Conf.*, 2018, pp. 1–7.

[28] Y. Kagawa et al., "Development of face-to-face and face-to-back ultra-fine pitch Cu-Cu hybrid bonding," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf.*, 2022, pp. 306–311.

[29] J. J. Suarez Berru, S. Nicolas, N. Bresson, M. Assous, and S. Borel, "Demonstration of a wafer level face- to-back (F2B) fine pitch cu-cu hybrid bonding with high density TSV for 3D integration applications," in *Proc. IEEE 73rd Electron. Compon. Technol. Conf.*, 2023, pp. 97–102.

[30] S. Iacovo et al., "The unique properties of SiCN as bonding material for hybrid bonding," in *Proc. 7th Int. Workshop Low Temp. Bonding 3D Integration*, 2021, p. 38.

[31] S. Bao et al., "AlN-AlN layer bonding and its thermal characteristics," *ECS J. Solid State Sci. Technol.*, vol. 4, no. 7, pp. P200–P205, 2015.

[32] K.-C. Shie et al., "Hybrid bonding of nano-twinned copper/organic dielectrics with low thermal budget," in *Proc. IEEE 71st Electron. Compon. Technol. Conf.*, 2021, pp. 432–437.

[33] L. Mirkarimi et al., "The influence of Cu microstructure on thermal budget in hybrid bonding," in *Proc. IEEE 72nd Electron. Compon. Technol. Conf.*, 2022, pp. 162–167.

[34] D. Liu et al., "Low temperature Cu/SiO_2 hybrid bonding with metal passivation," in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2.

[35] Y. Xian, Y. Meng, L. Zhang, J. Zhang, H. Zhou, and J. Fang, "Improvement of CU-CMP EDP curves for different pattern density," in *Proc. China Semicond. Technol. Int. Conf.*, 2022, pp. 1–2.

[36] K. Tanwar et al., "BEOL Cu CMP process evaluation for advanced technology nodes," *J. Electrochem. Soc.*, vol. 160, no. 12, pp. D3247–D3254, 2013.

[37] T. Fukushima et al., "Oxide-oxide thermocompression direct bonding technologies with capillary self-assembly for multichip-to-wafer heterogeneous 3D system integration," *Micromachines*, vol. 7, no. 10, 2016, Art. no. 184.

[38] S. H. Christiansen, R. Singh, and U. Gosele, "Wafer direct bonding: From advanced substrate engineering to future applications in micro/nanoelectronics," *Proc. IEEE*, vol. 94, no. 12, pp. 2060–2106, Dec. 2006.

[39] Q. Kang, G. Li, F. Niu, and C. Wang, "Cooperative surface-activation strategy for low-temperature Cu/SiO_2 hybrid bonding," in *Proc. IEEE Int. Conf. Integr. Circuits, Technol. Appl.*, 2022, pp. 40–41.

[40] K.-C. Shie, A. M. Gusak, K. N. Tu, and C. Chen, "A kinetic model of copper-to-copper direct bonding under thermal compression," *J. Mater. Res. Technol.*, vol. 15, pp. 2332–2344, 2021.

[41] D. C. H. Yu, C.-T. Wang, and H. Hsia, "Foundry perspectives on 2.5D/3D integration and roadmap," in *Proc. IEEE Int. Electron Devices Meeting*, 2021, pp. 3.7.1–3.7.4.

[42] Applied Materials, "Heterogeneous integration /hybrid bonding," 2023. [Online]. Available: https://www.appliedmaterials.com/us/en/semiconductor/markets-and-inflections/heterogeneous-integration/hybrid-bonding.html

[43] J. J.-Q. Lu, D. Zhang, and P. Ramm, "Overview of bonding and assembly for 3d integration," in *Handbook of 3D Integration, Volume 3: 3D Process Technology*, P. Garrou, M. Koyanagi, and P. Ramm, Eds., Hoboken, NJ, USA: Wiley, 2014, pp. 261–278.

[44] D. Liu, P.-C. Chen, T.-C. Chou, H.-W. Hu, and K.-N. Chen, "Demonstration of low-temperature fine-pitch Cu/SiO_2 hybrid bonding by au passivation," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 868–875, 2021.

[45] K. N. Chen et al., "Morphology and bond strength of copper wafer bonding," *Electrochem. Solid-State Lett.*, vol. 7, no. 1, pp. G14–G16, 2004.

N