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A review of mechanism and technology of hybrid bonding

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Abstract

With the development of semiconductor technology, traditional flip-chip bonding has been difficult to meet the high-density, high-reliability requirements of advanced packaging technology. As an advanced three-dimensional stacked packaging technology, Cu-SiO_2 hybrid bonding technology can achieve high-density electrical interconnection without bumps, which expands the transmission performance and interconnection density of chips greatly. However, the investigation on Cu-SiO_2 bonding is far from mature, and many researchers are studying Cu-SiO_2 bonding passionately. There are many technologies that use different bonding mechanisms to achieve Cu-SiO_2 bonding, which will affect the bonding strength directly. We review the mechanism and research progress of Cu-Cu bonding, SiO_2-SiO_2 bonding. What is more, we summarize the comparison of bonding conditions and bonding strength of

various methods furtherly. According to the bonding mechanism, we propose some economical solutions for low-temperature Cu-SiO_2 hybrid bonding, with the aim of providing certain references for the further development of advanced semiconductor packaging.

Keywords: Cu-SiO_2 hybrid bonding; bonding strength; bonding mechanism; Cu-Cu bonding; SiO_2-SiO_2 bonding

Introduction

New technologies, such as artificial intelligence and autonomous driving, have placed higher demands on the packaging and integration of electronic devices [1]. And the development of integrated circuits has followed Moore's Law basically. The size of transistors has been reduced continuously, while the performance of chips has been improved. However, with the continuous reduction of transistor size, the critical dimension of the transistor has approached the physical limitation. Although reducing the size of transistors can improve the performance of integrated circuits, there are serious problems such as leakage, heating and power consumption caused by short channel effect. When the process node is higher, the improvement of each process node will bring a sharp increase in cost. And the change of technical nodes is slowing down gradually, but the direction of high performance integrated circuits is unchanged. According to the international semiconductor technology development roadmap [2], the future development of integrated circuit technology will focus on the following

two directions: Direction 1: Continue to follow Moore's Law to reduce the critical dimension of transistors, improve circuit performance and reduce power consumption, that is, More Moore; Direction 2: Develop in the direction of multiple types, extending Moore's Law, that is, More Than Moore. Three-dimensional (3D) integration is an important application direction of More Than Moore. 3D integration technology mainly includes 3D integrated circuit packaging, 3D Si integration, and 3D integrated circuit integration [3]. 3D integration circuit packaging technology mainly uses micro-bump and Through Silicon Via (TSV) technology to realize chip-to-chip interconnection, while 3D Si integration realizes bump-free interconnection [4]. With the development of packaging technology, the packaging pitch is getting smaller and smaller, and the short circuit and migration problems of bump materials are becoming more and more serious [5]. 3D Si integration technology, which only uses TSV technology and is bump-free, comes into being. TSV technology is put forward by william shockley in 1958 [6]. Until now, in the mature and advanced TSV process, the TSV size can reach 5-10 um, the TSV pitch can reach 10-20 μm, and the TSV depth can reach 50-100 μm. The TSV of smaller size (1-3 μm) and finer pitch (< 10 μm) is under investigation [7-9]. TSV technology is a huge step for 3D package. However, TSV has serious thermal mechanical reliability problems [10]. The most unfavorable one is the mismatched thermal expansion coefficient between dielectric materials and conductive materials, which will cause the serious thermal stress during the manufacturing process, leading to the device failure. On the other hand, the chip will produce a large amount of heat when working, which will

decrease the TSV reliability dramatically [11]. And when these problems occur in CMOS images sensor [12], high bandwidth memory [13], active pixel transmission sensors [14], which require high-density TSV interconnects, the problem of thermal stress is more serious in times of crisis.

Hybrid Bonding (HB) is the key method for 3D Si integration technology. Hybrid bonding is a permanent bonding that combines dielectric materials and embedded metal to form an interconnection, as shown in Fig. 1, where the metal generally refer to Cu, Al, Au, and the dielectric materials generally refer to SiO_2, SiCN or polyimide. Different with traditional wire bonding and flip chip packaging (minimum interconnect pitch 20-50 μm) [15], hybrid bonding technology is connected by metal-metal bonding and dielectric-dielectric bonding directly, instead of introducing wire or micro-bump [16-20]. dielectric-dielectric bonding can provide mechanical support and electrical isolation for the entire integrated circuit, and metal-metal bonding can realize the vertical interconnection of the chips. For this reason, hybrid bonding technology enables ultra-high-density electrical interconnections (interconnect pitch less than 5μm) [21-25].

Due to the superiority of hybrid bonding technology, the international leading semiconductor manufacturers are developing hybrid bonding technology vigorously. Hybrid bonding technology has been applied to CMOS image sensors, high-bandwidth memory, and other devices gradually [26-30]. This technology has been used in artificial intelligence, camera, high performance computing and so on [30-32]. SONY used the hybrid bonding technology to realize the connection of 90 nm CIS

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chip and 65 nm logic chip [26-27], as shown in Figure 2. But on the other hand, hybrid bonding technology still faces many challenges, the most important is that metal-metal bonding and dielectric-dielectric bonding mechanism is different, which need to develop compatible bonding technology; Secondly, the bonding process usually requires the use of high-temperature process, which will cause thermal impact on the device, so it is necessary to develop thermal management technology. In addition, from the perspective of mass production, bonding strength, wafer deformation and bending, bonding alignment, manufacturing throughput, detection, reliability all needs to be improved. And bonding strength is the key parameter for hybrid bonding. Improving the bonding strength of metal-metal and dielectric-dielectric is the only way to improve the overall bonding strength. Since Cu and SiO_2 is the most compatible materials for Si-based CMOS process, the most common combination for hybrid bonding is Cu-SiO_2. Therefore, in this paper, Cu-SiO_2 hybrid bonding is taken as an example. We summarize the bonding mechanisms of various methods for Cu-Cu bonding, SiO_2-SiO_2 bonding and the technologies combining of Cu-Cu bonding and SiO_2-SiO_2 bonding. In addition, we have proposed some technologies to improve the Cu-SiO_2 hybrid bonding strength by comparing the Cu-Cu bonding, SiO_2-SiO_2 bonding technology. The properties of bonding materials, thermal management and reliability are also critical to the bonding quality, so these key factors are also discussed in this review paper in order to provide some references for improving the bonding quality.

Cu-Cu bonding mechanism and technologies

The traditional Cu-Cu bonding method is thermo-compression bonding, that is, by applying external pressure and under the condition of certain temperature, promoting the diffusion of copper atoms at the bonding interface to form Cu-Cu metallic bond. Jang et al. [33] compared the interface of Cu-Cu thermo-compression bonding at 300℃, 350℃ and 400℃ under the pressure of 25 KN. The results are shown in Figure 3. They found out that the temperature needs to reach at least 400℃ to obtain a rather better Cu bonding interface. And the interfacial adhesion energy was 4.93 J/m^2. After bonding at the temperature of 300℃, then annealing at 300℃ in N_2 atmosphere for 1h, it can also improve the bonding strength effectively, and the bind energy of the interface can reach 10 J/m^2.

High-temperature heating and high-temperature annealing for a long time are easy to produce thermal-stress, resulting in the deformation and the fracture of the device, which will cause the chip failure [34-36]. In addition, high temperature will raise higher requirements for equipment [37]. In order to prevent excessive deformation or damage to the chip, low temperature Cu-Cu bonding is needed. Low temperature bonding can improve the thermal migration, thermal stress induced warping, offset and other problems obviously, which will improve the reliability of device substantially [38-39]. Low temperature bonding will reduce the bonding energy, resulting in low bonding strength and low reliability of the chip [40-41]. In order to achieve excellent bonding performance at low bonding temperature, researchers have proposed many optimization schemes for Cu-Cu bonding.

First of all, a good Cu-Cu bonding interface can be obtained at a low bonding temperature by choosing a suitable Cu matrix structure to obtain a higher diffusion rate of copper [42-46]. Liu et al. [42] found that at the temperature of 150-300℃, the diffusion rate of Cu atom on the (111) plane is 3-6 orders of magnitude higher than that on the (100) and (110) planes, as shown in Table 1. Direct Cu-Cu bonding was achieved at temperature of 200 °C using a compressive pressure of 100 psi (0.69 MPa) held for 60 min at 10^{-3} tort, and the bonding strength reached 4.3 MPa. Han et al. [44] found that the high-density defect Cu (HD Cu) prepared by electroplating under high current condition at 0℃, polished by 85% phosphoric acid and cleaned with citric acid, can be well bonded at the temperature of 240℃ under the pressure of 80 MPa in N_2 atmosphere for 60 min by the method of thermo-compression bonding, while the normal Cu bonding interface was still obvious under the same bonding conditions, as shown in Figure 4. This is because there are many defects and stress-strain bands inside the high-density defect Cu. During the Cu bonding process, the stress-strain energy is released, promoting diffusion and accelerating bonding. Wang et al. [45] found that nanocrystal line Cu (NC-Cu) has higher diffusion rate than coarse-grained Cu (Cg-Cu), and it is easier for nanocrystal line Cu to grow up at low temperature. Thus, nanocrystal line Cu can be well bonded by thermo-compression bonding at the temperature of 250℃ under the pressure of 10 MPa at the vacuum of 0.05 Pa for 60 min, as shown in Figure 5. However, the bonding of nanocrystal line Cu has high requirements on surface roughness, and nanocrystalline Cu is easily oxidized. Chou et al. [46] proposed the pillar-concave structure for Cu-Cu direct bonding. that is, the

protruding structure of Cu is inserted into the concave structure of Cu, as shown in Figure 6. At the temperature of 150℃ and under the pressure of 200N, or 200℃ and 100N, a good bonding interface can be obtained within only 1min. This is due to the plastic deformation of Cu on the protruding and concave structure, and the thermal effect generated by the plastic deformation accelerates the diffusion of Cu atoms on the interface.

Secondly, a good Cu-Cu bonding interface can also be obtained through surface treatment. Many researchers have realized low temperature Cu-Cu bonding by formic acid treatment [47-49]. Jangam et al. [47] can realize Cu-Cu bonding in 5s using In-situ formic acid vapor treatment at the temperature of 240℃ under the pressure of 250 MPa, and the average bonding strength can reach 150 MPa, as shown in Figure 7. The principle is that the introduction of formic acid can remove the oxide of the bonding interface effectively: CuO on the Cu interface surface reacts with formic acid to generate copper formate, and copper formate decomposes into Cu, the chemical reaction equation is as follows:

$$2HCOOH\,(g) + CuO\,(s) \rightarrow (HCOO)_2Cu\,(s) + H_2O\,(g) \quad (1)$$

$$(HCOO)_2Cu(s) \rightarrow Cu\,(s) + 2CO_2\,(g) + H_2\,(g) \quad (2)$$

Another well-reported method is surface activated bonding (SAB) [50-53]. Surface activated bonding uses plasma to bombard the Cu surface in an ultra-high vacuum (10^{-6} Pa) to remove oxides and other contaminants from the copper surface physically, and then form a Cu-Cu bonding at room temperature. The surface activated treatment and the entire bonding process all complete in a high vacuum environment. Kim et al.

[50] used Ar Plasma pretreatment to realize Cu-Cu direct bonding at room temperature under pressure of 1000 kgf and ultra-high vacuum of 10^{-8} torr, and its bonding strength was above 6.47 MPa. Park et al. [52] used Ar/N_2 two-step plasma surface treatment to achieve Cu-Cu direct bonding with bonding strength of 62.6 MPa at 0.9Mpa and 260℃.

Some experts have also proposed the method of using Ti [54], Ag [55-56] and other metals to deposit passivation layers on the surface of copper. The main function of the metallic passivation layer on the surface of Cu is to protect Cu from oxidation. In addition, to a certain extent, it can reduce the roughness of the bonding interface. During the bonding process, Cu diffuses towards the bonding interface and forms diffused copper at the bonding interface. The bonding mechanism is shown in Figure 8. Panigrahi et al. [54] deposited an ultra-thin Titanium (Ti) passivation layer (3 nm). Under the condition of 160℃ and 2.5 Bar, a large amount of Cu grain growth can be observed, which indicates that there is an obvious diffusion of copper across the boundary to complete Cu-Cu bonding. Similarly, Tan [57], Peng [58] et al. proposed a method for passivation of self-assembled monolayer (SAM). Self-assembled molecular layer passivation can also protect the Cu to be bonded from oxidation effectively, but its bonding process is different from metallic passivation layer. The wafer is soaked in an alkane-thiol solution, then an organic passivation layer is formed on the surface of the Cu to be bonded, and the organic passivation layer is removed by sintering for 10 minutes in a nitrogen atmosphere at 250℃, and then Cu-Cu bonding is carried out. Tan et al. [57] used the method of self-assembled

molecular passivation layer to perform Cu-Cu bonding at 250℃ and 2500 mbar vacuum for 1h. The bonding interface without passivation protection was still obvious, and under the protection of passivation layer, the bonding interface showed a clean bonding morphology. A large number of Cu grains grow, and the Cu grains cross over the original bonding interface to form a solid Cu-Cu bonding, as shown in Figure 9.

In 2021, Hung et al. [59] proposed using wet chemistry for pretreatment to remove oxidations on the bonding surface at the 71st electronic components and technical conference. By comparing the Cu-Cu bonding results after citric acid, sulfuric acid, hydrochloric acid and acetic acid pretreatment, it is found that pores of the sample on the bonding interface after citric acid treatment are smaller and fewer. correspondingly, the shear strength of the sample treated by citric acid is also higher after Cu-Cu bonding. The measured values of the pull test results are 5.57, 8.98, 8.16, and 7.51 MPa for the pretreatment of acetic acid, citric acid, sulfuric acid, and hydrochloric acid, respectively.

Moreover, Qiu et al. [60] proposed an ultrasonic bonding technology, the principle of which is that the high-frequency vibration of ultrasonic waves causes deformation of the surface of Cu to be bonded and destroys the oxide layer on the surface. This technology has no strict requirements for the flatness and roughness of the surface of bonded Cu, and realizes the Cu-Cu bonding at room temperature, and the bonding strength increases with the increase of vibration amplitude.

In addition to Cu-Cu direct bonding, many researchers have also conducted in-depth research on Cu-Cu indirect bonding. Cu-Cu indirect bonding is to add

auxiliary materials between the Cu to be bonded to form a more effective Cu-Cu bonding. Du et al. [61] achieved Cu-Cu bonding at 150℃ and 10 MPa by growing Cu nanowires on the surface of the Cu to be bonded, and the bonding strength was greater than 15 MPa. Liu et al. [62] prepared Ag nanostructures on the surface of Cu to be bonded, and completed Cu-Cu bonding in only 5 min at 250℃ and 20 MPa in a N_2 atmosphere. The bonding strength reached 14.4 MPa after annealing in a vacuum furnace at 250℃ for 25 min. Cu-Cu indirect bonding based on Cu nanowires or Ag nanostructures can achieve low temperature Cu-Cu bonding, but its preparation method is complex and not suitable for large-scale production.

SiO_2-SiO_2 bonding mechanism and technologies

Unlike the Cu-Cu bonding which mainly depends on the diffusion of Cu atoms, the SiO_2- SiO_2 bonding process can be divided into hydrophilic bonding and hydrophobic bonding according to the surface morphology of SiO_2 to be bonded. the bonding which forms hydrophilic groups (-OH) on the surface of SiO_2 to be bonded is hydrophilic bonding. SC1 solution or SPM solution is usually used to treat the SiO_2 surface for pre-treatment [63]. The bonding which forms hydrophobic groups (Si-H) on the surface of SiO_2 to be bonded is hydrophobic bonding, and HF solution is usually used to pretreat the bonded SiO_2 surface [64].

Gösele et al. [65] compared the surface energy of hydrophilic bonding and hydrophobic bonding with the annealing temperature and found that the annealing temperature of hydrophobic bonding needs to reach 600℃ to obtain the required

bonding strength, while the annealing temperature of hydrophilic bonding only needs 200℃ to achieve the required bonding strength, as shown in Figure 10. Therefore, SiO_2 hydrophilic bonding is the mainstream method at present.

The basic principle of hydrophilic bonding is that the chemical reaction take place between the hydroxyl groups attached to the surface of the hydrophilic wafer to form covalent bonds. Figure 11 shows the classical four-stage mechanism model of SiO_2 hydrophilic bonding proposed by Tong et al. [66]. The model indicates that silanol groups (≡Si-OH) and water molecules attached to the smooth and clean surface of silicon wafer are mainly involved in the bonding process. In the first phase of the bonding process, the silicon wafer is bonded to each other by hydrogen bonds between water molecules, as shown in Figure 11(a). After annealing at the temperature of 110~150℃, the silanol groups between the silicon wafer reacts with each other to form the silicon-oxygen-silicon covalent bond (≡Si-O-Si≡), so as to achieve the bonding, and some silanol groups are still retained, the reaction equation is as follows:

$$\equiv Si\text{-}OH + HO\text{-}Si\equiv \rightarrow \equiv Si\text{-}O\text{-}Si\equiv + H_2O \qquad (3)$$

In this stage, at the interface of silicon wafer, water molecules are formed and diffuse outward, as shown in Figure 11(b). At the same time, some formed water molecules will spread through the natural oxide layer to the inside of the silicon wafer, and react with the silicon wafer to produce hydrogen:

$$H_2O + 2 \equiv Si\text{-} \rightarrow \equiv Si\text{-}O\text{-}Si\equiv + H_2 \qquad (4)$$

At the temperature of 150-800℃, the silanol groups can be completely converted into

silicon-oxygen-silicon covalent bonds, as shown in Figure 11(c). In this process, the bonding strength is mainly affected by the contact area of the silicon wafer. When the temperature is higher than 800℃, the viscous flow occurs and the bonding strength reaches the maximum, as shown in Figure 11(d).

The classical four-stage mechanism model of hydrophilic bonding does not consider the roughness of the surface. Liao et al. [67] analyzed the influence of surface energy and surface topography on bonding, and proposed a bonding contact model considering the surficial characteristics of the wafer, as shown in Figure 12. During the bonding process, the surface topography of the wafer is deformed, the contact area of the two surfaces increases, and the number of covalent bonds increases. The water molecules sandwiched in the bonding interface can cause internal stress corrosion on the surface of silicon or silicon dioxide, softening the concave and convex morphology of the wafer surface, which can improve the bonding quality. However, the precondition for the improvement of bonding quality is the control of the weight of water molecules. Too many water molecules at the interface are difficult to be removed by low temperature annealing completely, which is easy to lead to interface corrosion and cause holes. In addition, under the condition of the absence of a water-blocking layer, excess water molecules are easy to diffuse into the inside of the silicon wafer, which will react with silicon to generate hydrogen, resulting in a large number of bubbles to reduce the yield of SiO_2-SiO_2 bonding.

According to the classical four-stage mechanism model, increasing the hydroxyl groups and controlling the suitable water molecules on the bonding interface can

improve the bonding quality. Zhao et al. [68] compared the bonding strength between the wafer treated by 29% ammonia and those without ammonia. They found out that the bond rate of wafers treated by ammonia reached over 95% and the bonding strength reached 7.2MPa, while the bond rate of wafers treated without ammonia was only 80% and the bonding strength was only 3.1MPa, as shown in Figure 13. It is suggested that the use of ammonia treatment can create more Si-OH groups on the wafer surface, which can enhance the surface bonding energy. According to the classical four-stage mechanism model of SiO_2-SiO_2 hydrophilic bonding, Si-O-Si covalent bonds are generated during the bonding process. After ammonia treatment, while hydroxyl is produced, a large number of silanol groups are converted into Si-NH2 groups, which all contribute to the completion of low-temperature bonding. The reaction is as follows:

$$\equiv Si\text{-}OH + NH_3 \cdot H_2O = \equiv Si\text{-}NH_2 + 2H_2O \qquad (5)$$

Plasma surface treatment is also an effective way to improve SiO_2-SiO_2 bonding. He et al. [69] found that the Si containing Ar plasma treatment can not only remove the pollutants on the surface to be bonded, but also enrich a layer of silicon on the wafer surface, as shown in Figure 14. the silicon-rich surface contains more Si-Si bonds and suspended Si bonds, also known as oxygen vacancy defects, which greatly promotes the adsorption of hydroxyl groups on the surface to be bonded. This results in an increase of silanol groups, and causes the increases of the bonding strength. At present, the annealing temperature of hydrophilic bonding can be reduced to 200℃ by using plasma surface treatment.

Technologies combining of Cu-Cu and SiO_2-SiO_2 bonding

Actually, the bonding process always combines of Cu-Cu and SiO_2-SiO_2 bonding. Direct Bond Interconnect (DBI) is a bonding technology proposed by Ziptronix in 2009 firstly [70]. The bonding process is shown in Figure 15. After forming Damascus grooves on the wafer, the copper is electrical plated and then polished using a chemical mechanical polishing (CMP) process to obtain a clean and smooth surface to be bonded. Then, hydrophilic groups are obtained by N_2 plasma activation to achieve good SiO_2-SiO_2 bonding surface, and Cu-Cu metal interconnect is realized under the condition of low temperature annealing at 125-400℃ finally.

In DBI technology, CMP process is particularly important. The main function of CMP process is to grind off the excess Cu and achieve the flat surface without damage, but there are often many problems in the actual CMP process. The most common problem is dishing because of the different polishing rate between Cu and SiO_2, as shown in Figure 16, which leads to the SiO_2- SiO_2 contact, while Cu-Cu cannot contact directly, that is to say, only the SiO_2 interface achieves bonding, while there is a gap between the Cu-Cu interface. In addition, the defect will also lead to the low quality of the hybrid bonding, such as oxide, pollution, void and so on. Sierra-Suarez et al. [71] found that in the final stage of CMP process, Cu and exposed tantalum would be subjected to galvanic corrosion in the polishing slurry, which makes the low quality of hybrid bonding. They proposed that corrosion could be inhibited by adding benzotriazole (BTA) to reduce Cu defects. SEM images of the different concentrations between 0.005 - 0.1% by weight in the copper plugs are

shown in Figure 17. the addition of BTA increased non-uniformity and decreased the material removal rate of Cu, while the BTA is effective at curtailing the corrosion of the copper ultimately. Additionally, the dishing of copper increased, potentially due to the non-uniformity and particle agglomeration caused by impacting particle dispersion stability with a non-optimal component balance. This may be alarming at first, since there is a limit to the amount of dishing tolerable by the DBI process, but it can be compensated for during the barrier polish with careful control of the selectivity and duration. The ideal solution is to introduce the BTA after the bulk copper has cleared. The galvanic corrosion can be forbidden when the BTA concentration reaches 0.1%.

Because the thermal expansion coefficient of Cu is higher than that of silicon oxide, the diffusion of Cu can be accelerated by annealing treatment, and the bonding of Cu interface with Cu gap heights can also be realized. Mudrick et al. [72] studied the relationship among the bonding strength, Cu gap heights and the annealing temperature. The results are shown in Fig. 18. They found out that when Cu gap height is between 18-32 nm, bonding can be achieved at 250℃, and the resistance decreases with the increase of annealing temperature. When the Cu gap height is 9 nm, the annealing temperature must reach 350℃ or above in order to form effective connections.

He et al. [73] proposed a bonding method using Si-containing Ar plasma activation. SiO_2-SiO_2 bonding can be promoted by using Si-containing Ar plasma. After plasma activation, hybrid bonding can be realized by two process routes, one is bonded at

room temperature under ultra-high vacuum of 5×10^{-6} Pa directly, and the other is realized by preprocess-pre-bonding-separation-final bonding, as shown in Figure 19. Although the process route of pretreatment-pre-bonding-separation-final bonding is more complex, the bonding strength is higher than that of direct bonding under ultra-high vacuum, because the adsorption of hydroxyl groups and removal of surface water molecules before the final bonding, which can improve the bonding strength and reduce the interface voids. At the same time, the oxygen content of Cu-Cu bonding interface can be reduced effectively.

Seo et al. [74] used Ar and N_2 two-step plasma treatment to achieve hybrid bonding. The XPS diagram shows that Cu_4N is generated after N2 plasma treatment, as shown in Figure 20. Cu_4N can protect the Cu bonding surface from oxidation effectively, and the surface has a higher electrical conductivity. In addition, the Si-N bonds formed by N2 plasma treatment are more conducive to medium bonding [75]

Comparison of various bonding Technologies for Cu/SiO_2 bonding

This paper summarizes various methods used for Cu-Cu bonding, SiO_2-SiO_2 bonding technologies in recent years, and the comparison of bonding conditions and bonding strength of various methods is summarized in Table 2.

The traditional Cu-Cu thermo-compression bonding process can be achieved at 400°C, but there are two main problems. First, the copper process is not suitable for high temperature process, which is easy to cause copper diffusion, resulting in device failure. The second is that the bonding strength achieved only by

thermos-compression bonding process will be relatively low, which cannot meet the requirements of applications. To prevent device failure, researchers began to study the low-temperature bonding process.

Many technologies can achieve low temperature bonding in the laboratory, but they are not suitable for mass production. The method of increasing the diffusion rate of copper by preparing HD-Cu or nanocrystalline copper is not suitable for actual production, which not only complicates the process and increases the cost, but also is not suitable for large-scale mass production. The pillar concave bonding method can realize the low-temperature bonding quickly and does not require CMP processing. Instead, it requires the structure of pillar and concave, which increases the complexity of the process. Meanwhile, its principle is to promote bonding by deformation, so extreme pressure is needed to achieve bonding. This is not easy to control in actual production, and it is easy to cause damage to the device. Low-temperature bonding can be achieved quickly in a short time by injecting formic acid vapor, but there are many difficulties in actual production. On the one hand, the need of very high gas flow rate (500~1,000 L/min) is difficult to achieve, and the high flow tare is easy to generate static electricity and stress; on the other hand, the introduction of formic acid vapor needs very high requirements for equipment. The introduction of passivation layer, self-assembled monolayer and indirect bonding requires the introduction of other materials, and the process is complex, which leads to high cost, low yield, and it is difficult to realize large-scale mass production. The use of ultrasonic bonding can achieve low temperature bonding in a short time, but the surface of the wafer is

required to have good flatness. The process operation and equipment requirements are higher. In addition, the higher hardness of copper and the higher oxidation rate make the bonding more difficult. The technical challenges, mechanisms and solutions of each bonding technologies, including Cu-Cu bonding, SiO_2-SiO_2 bonding technology as well as Cu-SiO_2 bonding, are summarized in Table 3. For Cu-Cu bonding, there are two bonding mechanisms: increasing the diffusion rate of Cu and cleaning the surface to be bonded. For SiO_2-SiO_2 bonding and Cu-SiO_2 bonding, the bonding mechanism is surface treatment. The solutions to improve bonding quality are various, such as low temperature bonding, using (111) plane directly, equipment improvement, process parameter optimization, Q-Time control, and so on.

And some technologies can be applied to mass production. By adjusting the crystal direction of the wafer to increase the diffusion rate of copper, the bonding temperature can be reduced effectively to achieve low temperature bonding, which is still one of the effective means to achieve low temperature bonding in actual production. Wet chemical pre-treatment is a commonly used technical means. The wafers are often cleaned by wet chemical before processing, but the main problem of this method is that after wet chemical treatment, the wafers have to be taken out of the working chamber to wait for the next process, resulting in the surface re-oxidized easily. Plasma surface activation is a relatively mature technology at present, the equipment can generate plasma, bombard the wafer, and perform surface treatment, and then carry out the next process directly.

It can be seen that among the technical methods compatible with Cu and SiO_2,

combined with the actual production, equipment and process requirements, the better bonding strength and other dimensions, plasma surface activation is the most suitable method to achieve hybrid bonding.

Other key factors affecting bonding quality

In this review paper, we have discussed various bonding technologies and mechanisms. Not only the various bonding technologies are critical to the bonding quality, but also the properties of materials, thermal management, reliability and so on.

For the hybrid bonding, the properties of materials are very crucial. the electrical conductivity is the most critical, so the Au, Al and Cu can be chosen [76-87]. However, Au is too expensive and hard to process [76,77,84]. Al is easy to migrate, causing the void in the metal [78-79]. Therefore, Cu is the mostly selected conductor in HB. Another consideration is the machinability. The hybrid bonding requires a flat plane, the material should be able to be easily machined into a smooth surface. The thermal conductivity is also a key point. Hybrid bonding used for smaller pitch and more interconnections is sensitive to the thermal management. And thermal stability, electrical stability is important, which will affect the reliability [80-81]. The dielectric material should provide mechanical support and electrical isolation for the entire integrated circuit, so the mechanical property and insulating property should be rather better. The most critical property for dielectric material is compatible with the metallic material. The dielectric material such as SiCN [88-89], polyimide (PI) [84-85], SiO_2 [80-83]

has been investigated. Several current mainstream hybrid bonding materials are listed in Table 4.

The chip will produce a large amount of heat when working, so the thermal management is very critical for 3D packaging technology. The main heat dissipation channel generated is from the chip heat generation area to the outer surface of the device through the package structure, and then diffused to the surrounding environment through thermal convection and radiation. Therefore, the thermal management of 3D integrated circuits mainly involves three parts: heat source, heat conduction path and heat dissipation environment [88-96]. Men et al. used numerical and experimental method to improve heat distribution by topology optimization [90]. Mathew et al. designed deliberate channels for heat conduction [91]. Zhao et al. increased the content of materials with higher thermal conductivity to speed up the internal conduction [92]. Chen et al. used heat sinks for electronic chips [95]. The detailed main solutions of thermal management are summarized in Table 5.

The reliability is also a key parameter in 3D packaging technology. The most common failure modes reported for HB technologies are dielectric breakdown, copper diffusion in the dielectric, pad to pad misalignment, bonding voids and electromigration. The most common reliability threats, potential failures and solutions reported for HB technologies are listed in Table 6.

Conclusion

Three-dimensional integration is an important development direction of

integrated circuit technology in the future, and it is one of the key technologies to continue or even exceed Moore's Law. Cu-SiO_2 hybrid bonding technology can achieve vertical electrical interconnection and physical support without introducing bump simultaneously, and can achieve high-density and high-reliability three-dimensional integration. In this paper, we review the mechanism and research progress of Cu-Cu bonding, SiO_2-SiO_2 bonding. In addition, we summarize the comparison of bonding conditions and bonding strength of various methods furtherly. And put forward some key factors affecting bonding quality, such as the properties of materials, thermal management, reliability. According to the bonding mechanism, we propose some economical solutions for low-temperature Cu-SiO_2 hybrid bonding.

1. There are many technologies to achieve low temperature Cu-Cu bonding, such as selecting a suitable Cu matrix structure, Cu-Cu pillar-concave direct bonding, formic acid injection, surface plasma treatment, passivation layer, wet chemical treatment, and even ultrasonic treatment, but the principle is no more than two kinds: increasing the diffusion rate of Cu and cleaning the surface to be bonded.

2. The methods for achieving SiO_2-SiO_2 bonding can be divided into hydrophilic bonding and hydrophobic bonding, and hydrophilic bonding is the mainstream technology. Hydrophilic bonding can be achieved by wet chemical treatment or plasma treatment, the principle of which is to increase the hydroxyl group on the wafer surface and control the water molecule at the bonding interface.

3. Combined with current technology and research, Cu-SiO_2 hybrid bonding, which aims to be compatible with Cu-Cu bonding and SiO_2-SiO_2 bonding, can be

optimized by selecting (111) plane wafer, using wet chemical to clean wafer under the condition of controlling the process interval time. And the most suitable method to achieve hybrid bonding is plasma surface activation currently.

Cu-SiO_2 hybrid bonding technology has been applied in commercial mass production gradually, but Cu-SiO_2 hybrid bonding technology still has a lot of work to be done, including design and process parameter optimization, improving bonding accuracy, improving yield, reducing cost, thermal management and so on. There are also some work to be done from the perspective of theoretical research. At present, the main application of hybrid bonding is hydrophilic bonding. However, studies have shown that the hydrofluoric acid treatment of SiO_2 can obtain higher bonding strength than hydrophilic bonding. the hydrophobic bonding is worthy of further study. And various combinations of metals and dielectric materials will be expanded, not just Cu and SiO_2. With the development of hybrid technology, the hybrid bonding technology can not only be used in CMOS image sensors, high-bandwidth memory, artificial intelligence, camera, high performance computing, but also in high performance optoelectronic device, ultra-high density heterogeneous integration and so on. More efficient bonding technology and more advanced equipment development will promote the application of Cu-SiO2 hybrid bonding technology effectively.

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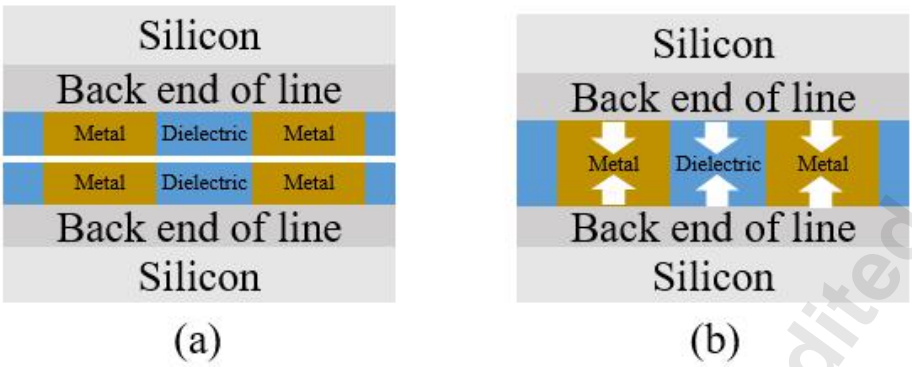

Fig. 1 Schematic of hybrid bonding (a) Dielectric material and embedded metal to be bonded (b) Dielectric material and embedded metal forming an interconnection after hybrid bonding

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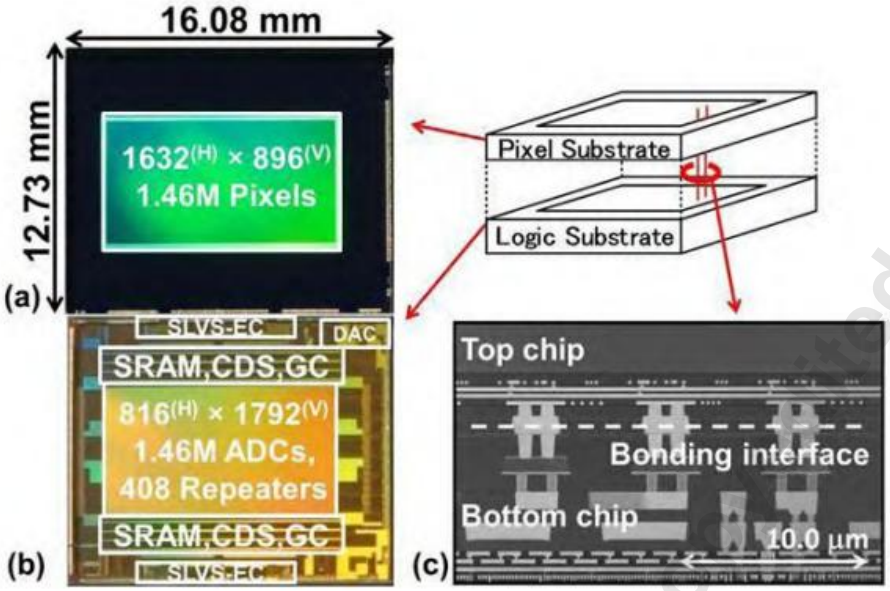

Fig. 2 Schematic of the connection of 90 nm CIS chip and 65 nm logic chip using SONY's hybrid bonding technology (a) CIS chip (b) logic chip (c) hybrid bonding cross section diagram [26]

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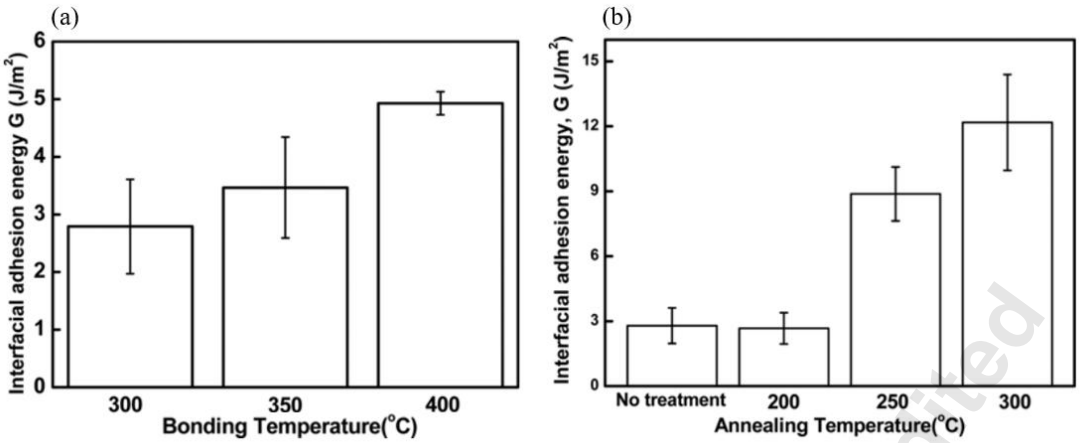

Fig. 3 (a) Changes of the interfacial adhesion energy between Cu-Cu bonded layer with bonding temperatures of 300℃, 350℃, and 400℃ for 60 min without annealing treatment (b) Changes of interfacial adhesion energy between Cu-Cu bonded layer with post-annealing temperatures at 200 ℃, 250℃, and 300℃ for 60 min [33]

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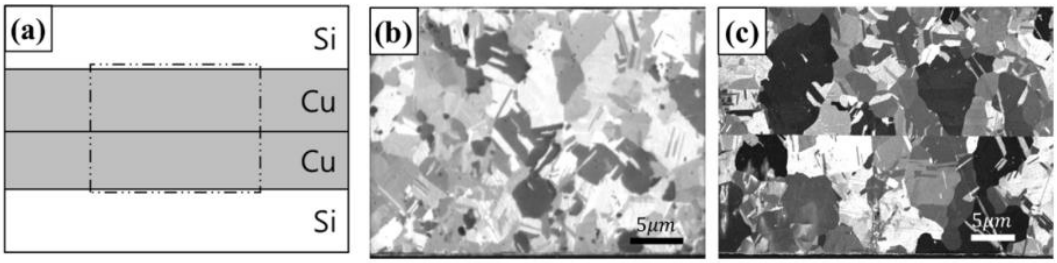

Fig. 4 HD Cu can be well bonded by the method of thermo-compression bonding, while the normal Cu bonding interface was still obvious under the same bonding conditions (a) Scheme of the Cu-Cu direct bonding. Vertical FIB images of the Cu-Cu direct bonding interface with (b) high defect density Cu and (c) normal Cu [44]

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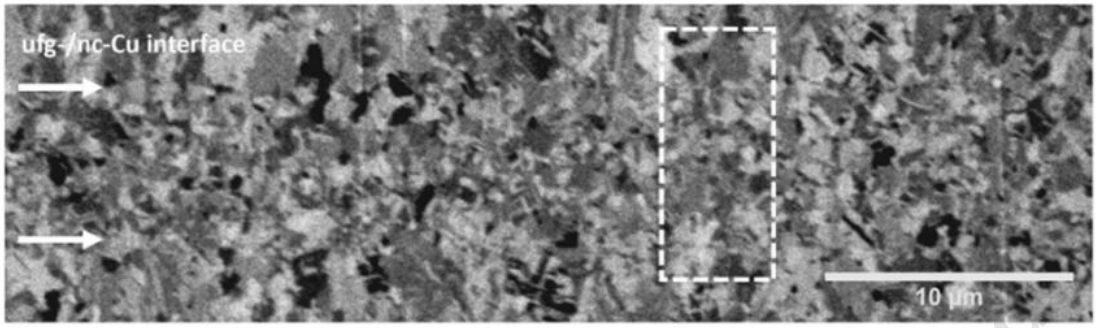

Fig. 5 SIM image of the overall interface of nc-Cu sample, SIM image show nc- Cu can be well bonded by thermo-compression bonding at the temperature of 250℃ under the pressure of 10 MPa at the vacuum of 0.05 Pa for 60 min [45]

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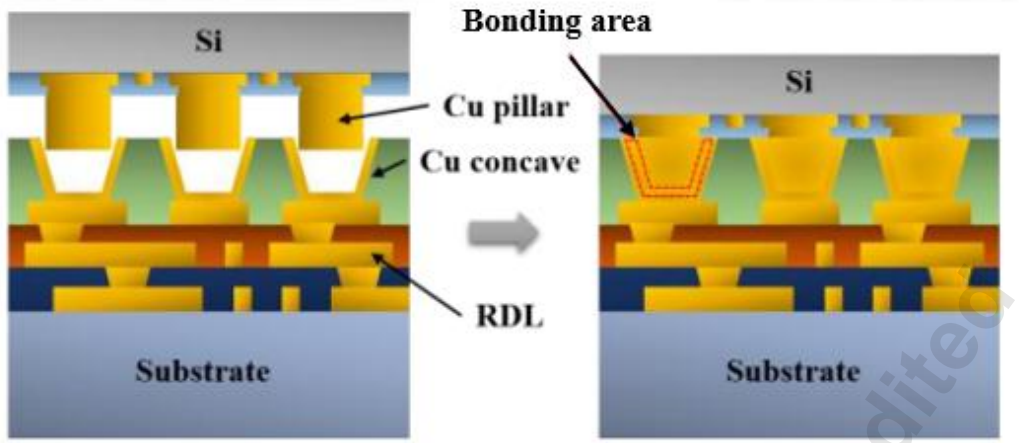

Fig. 6 Schematic of pillar-concave bonding, the protruding structure of Cu is inserted into the concave structure of Cu [46]

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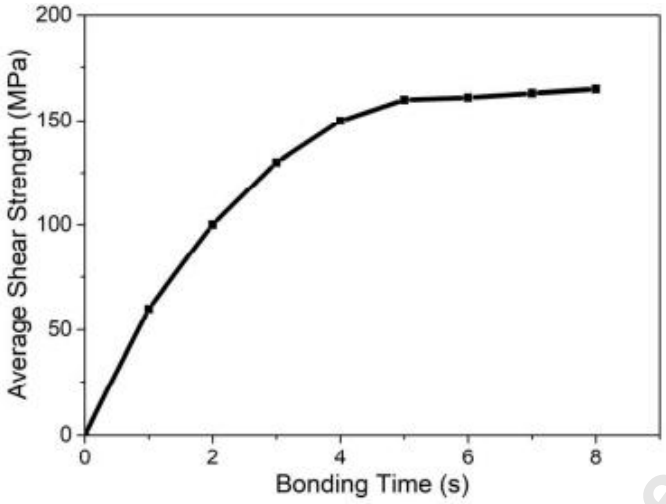

Fig. 7 Average shear strength vs bonding time for bonding pressure: 250 MPa and bonding temperature: 240 °C [47]

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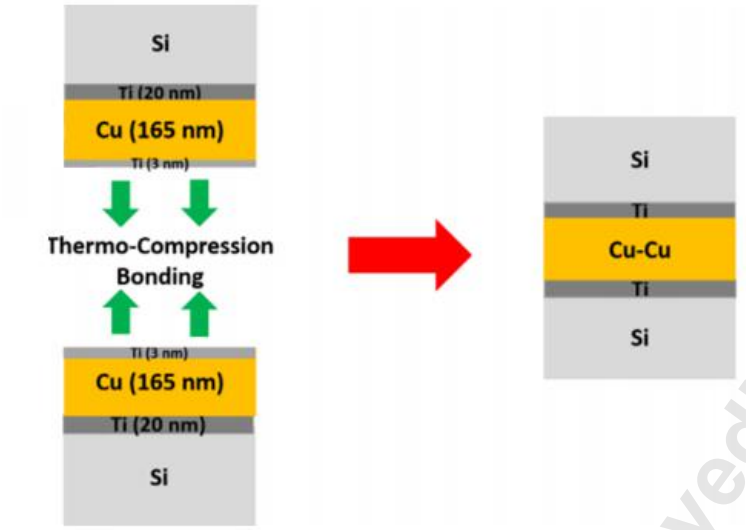

Fig. 8 Cu-Cu bonding mechanism of Ti passivation layer, Cu diffuses towards the bonding interface and forms diffused copper at the bondin4g interface [54]

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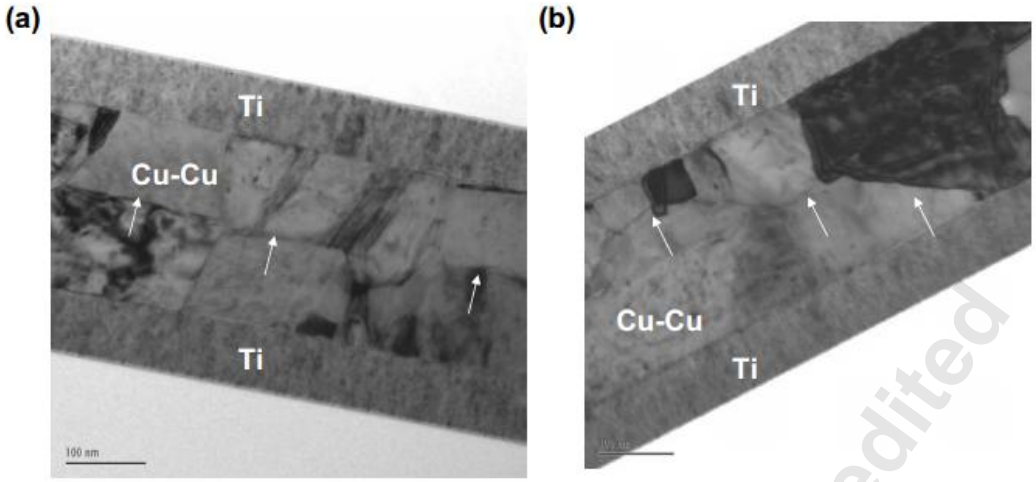

Fig. 9 TEM micrographs of bonded Cu layers, the bonding interface without passivation protection was still obvious, and under the protection of passivation layer, the bonding interface showed a clean bonding morphology. (a) without SAM passivation (b)with SAM passivation and desorption prior to bonding [57]

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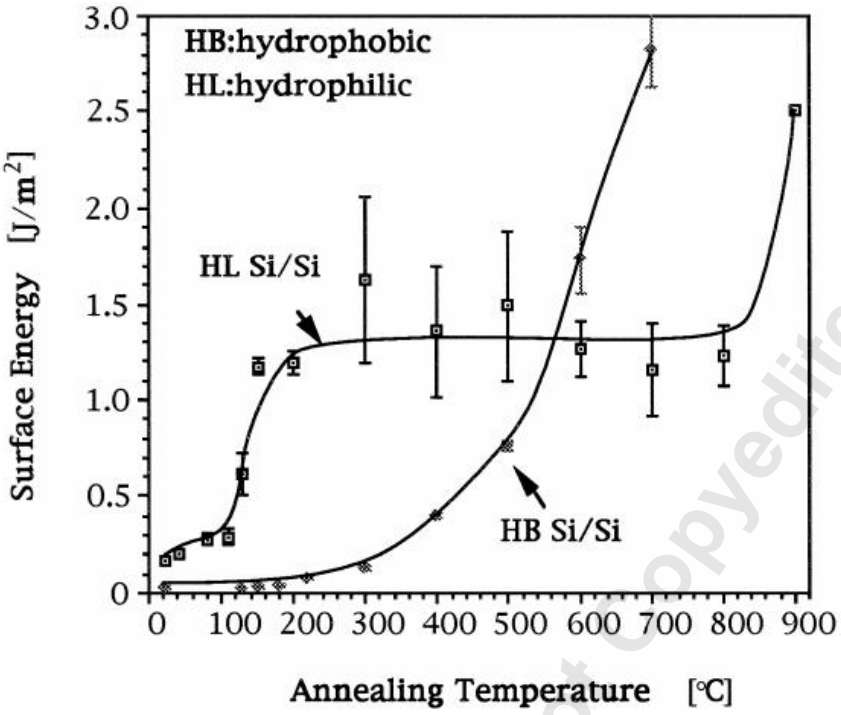

Fig. 10 surface energy of hydrophobic and hydrophilic bonding with annealing temperature, the annealing temperature of hydrophobic bonding needs to reach 600℃ to obtain the required bonding strength, while the annealing temperature of hydrophilic bonding only needs 200℃ [65]

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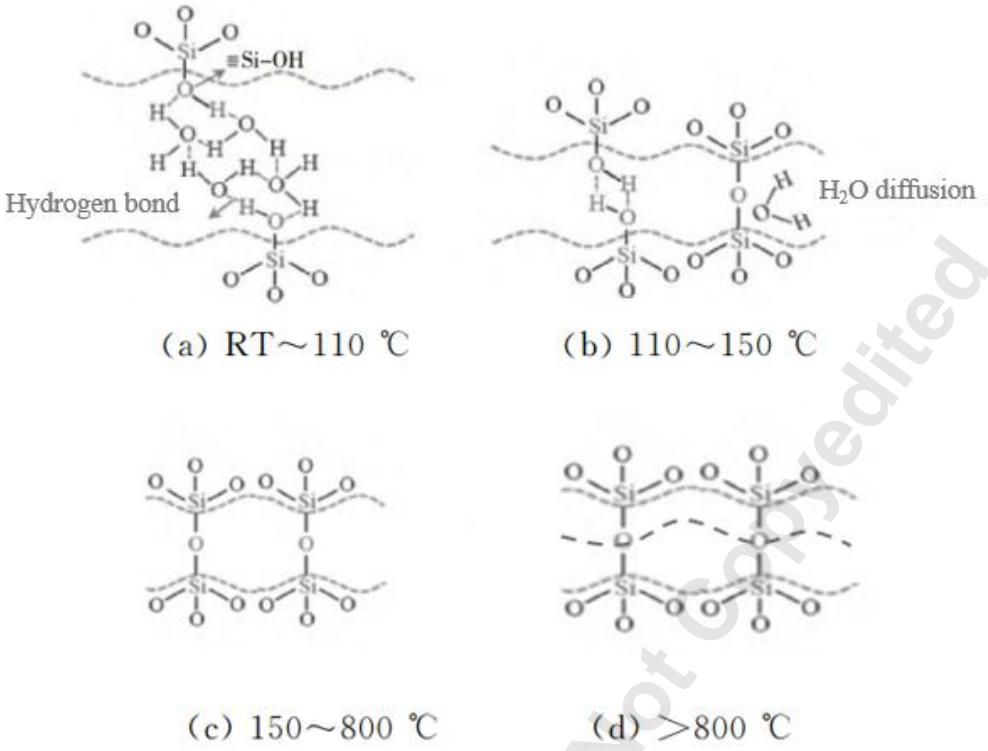

Fig. 11 Classical four-stage mechanism model of hydrophilic bonding [66]

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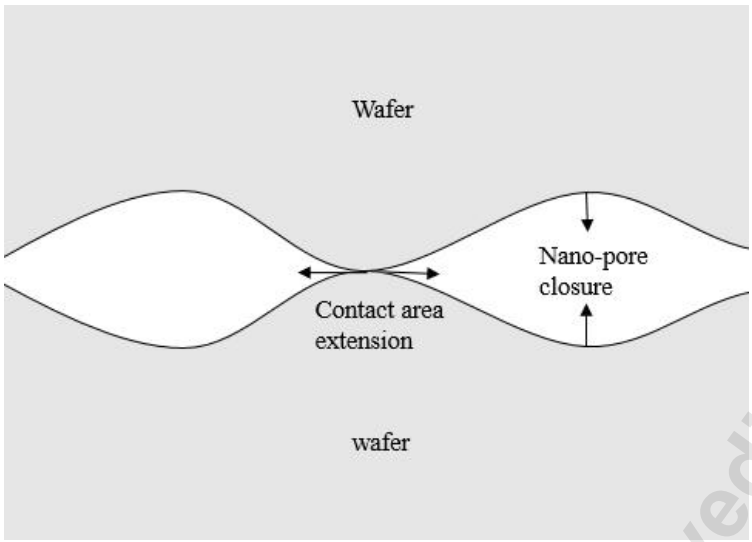

Fig. 12 Bonding contact model considering the surficial characteristics [67]

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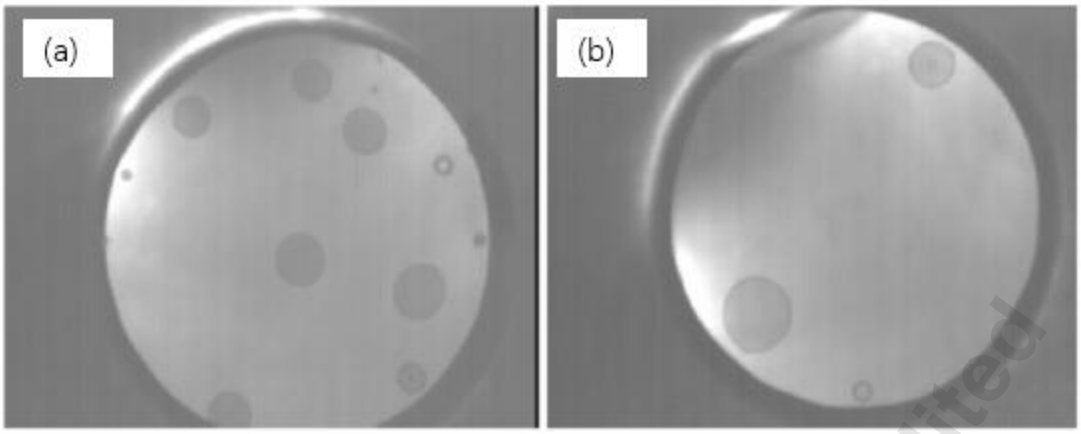

Fig. 13 Infrared transmission images of (a) without 29% ammonia treated and (b) 29% ammonia treated, the images show the bond rate of wafers treated by ammonia reached over 95% and the bonding strength reached 7.2MPa, while the bond rate of wafers treated without ammonia was only 80% and the bonding strength was only 3.1MPa [68]

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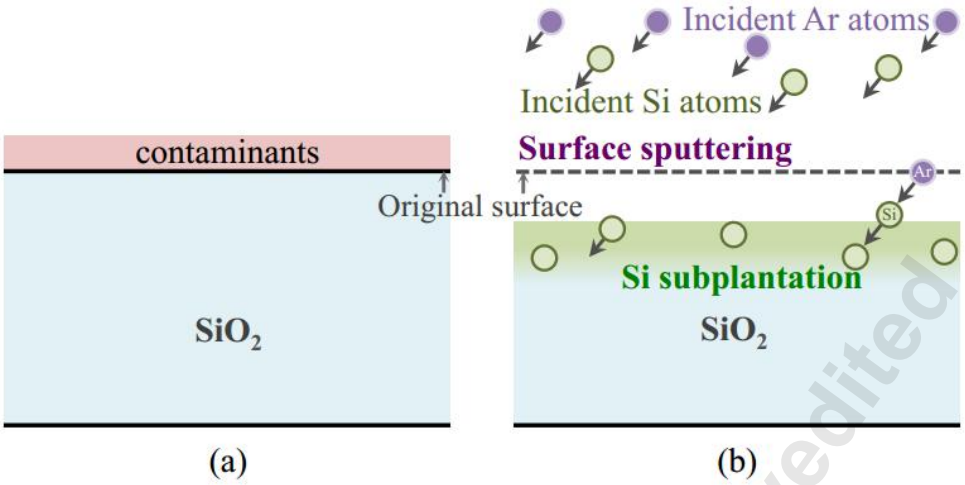

Fig. 14 Schematic representation of the Si-containing Ar beam irradiation on SiO_2 surface: (a) before irradiation and (b) after irradiation [69]

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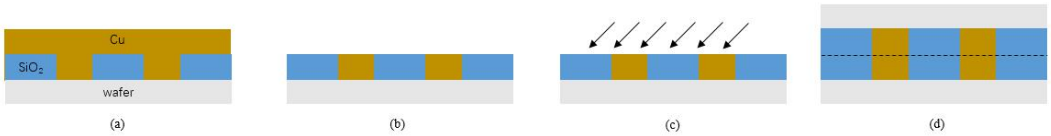

Fig. 15 DBI technology process, (a) form Damascus grooves, and electro-coppering. (b) CMP. (c) N_2 plasma to obtain hydrophilic groups. (d) SiO_2-SiO_2 bonding and Cu-Cu bonding [70]

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Fig. 16 chemical mechanical polishing (a) normal CMP and (b) dishing

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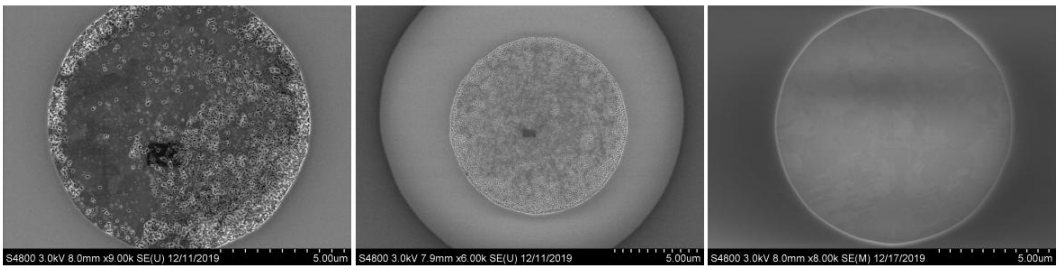

(a) +0.005% BTA (b) +0.02% BTA (c) +0.1% BTA

Fig. 17 galvanic Corrosion degree of different concentrations of BTA (a) 0.005% BTA. (b) 0.02% BTA. (c) 0.1% BTA [71]

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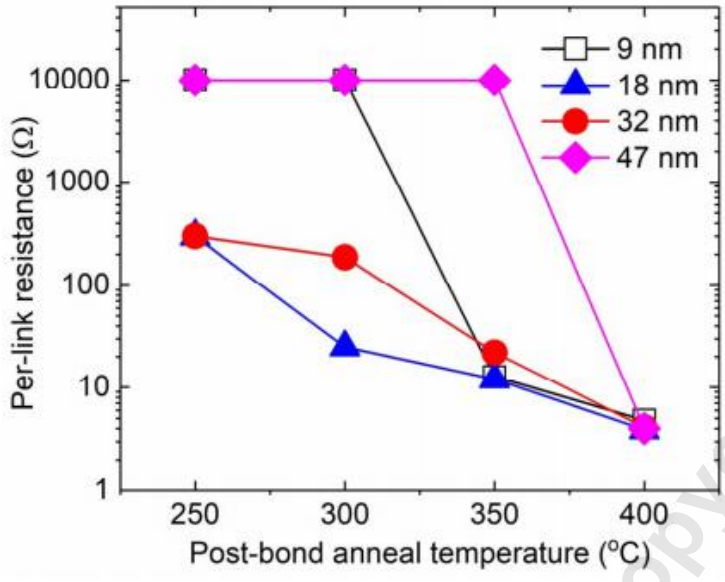

Fig. 18 Per-connection resistance as a function of post-bond annealing temperature for 4 different inter-die Cu-Cu gap heights [72]

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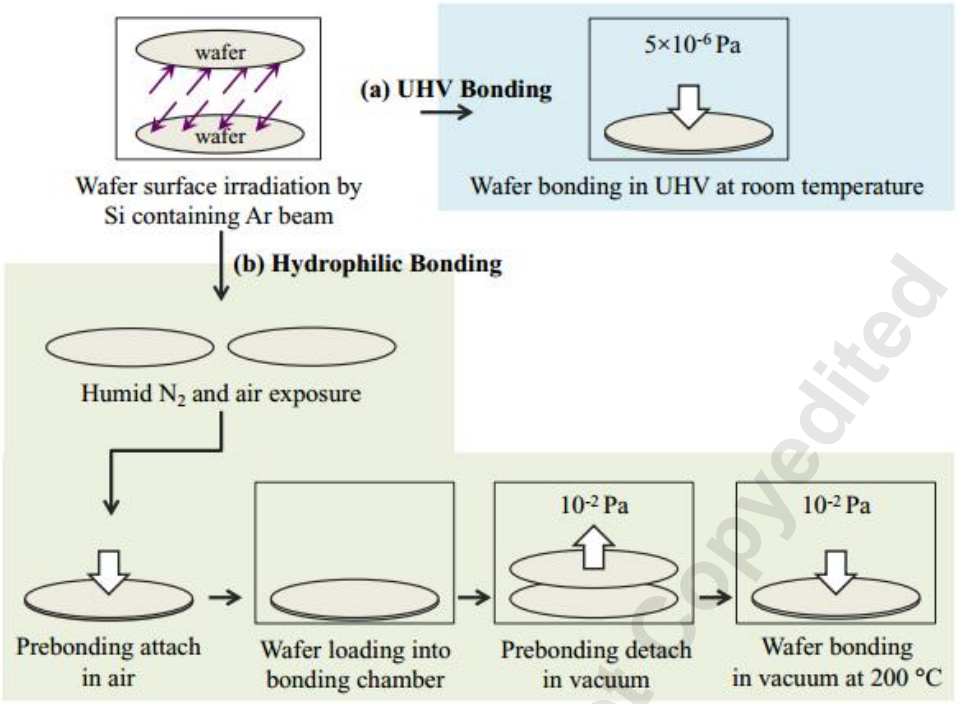

Fig. 19 Surface activation bonding process flow a) Direct bonding under ultra-high vacuum b) pretreatment - pre-bonding - separation - final bonding process [73]

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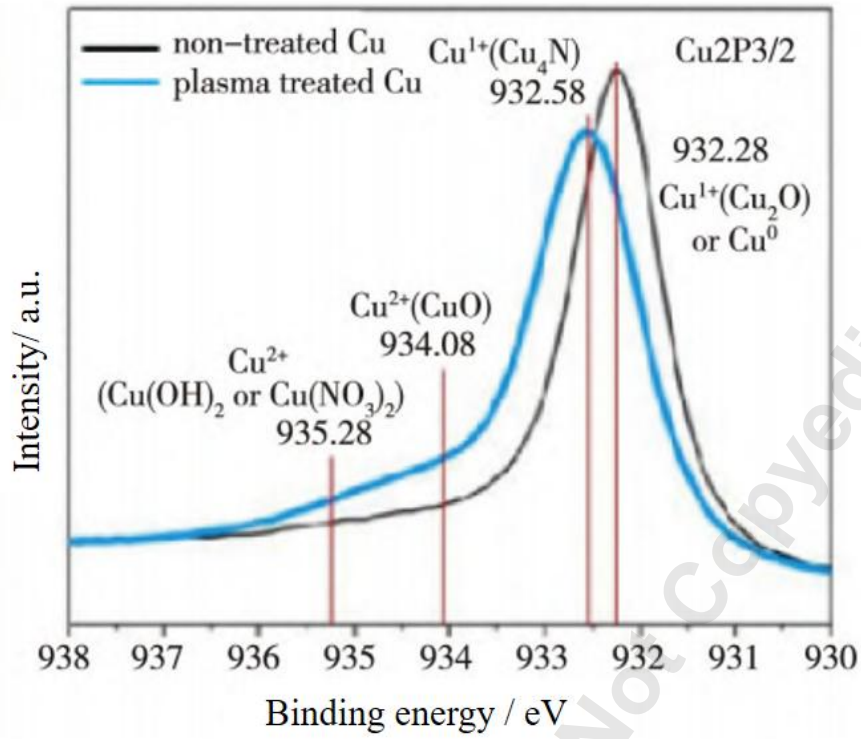

Fig. 20 XPS map of Cu surface after Ar and N_2 two-step plasma treatment, the XPS diagram shows that Cu_4N is generated after N2 plasma treatment [74]

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Table 1 Calculated Cu surface diffusivity (cm^2/sec) on (111), (100), and (110) planes at various temperatures [42]

$D_{surf.}$ \ Temp.	(111)	(100)	(110)
300℃	1.51×10^{-5}	1.48×10^{-8}	1.55×10^{-9}
250℃	1.22×10^{-5}	4.74×10^{-9}	3.56×10^{-10}
200℃	9.42×10^{-6}	1.19×10^{-9}	5.98×10^{-11}
150℃	6.85×10^{-6}	2.15×10^{-10}	6.61×10^{-12}

Table 2 Comparison of bonding conditions and bonding strength of different process

Bonding Material	Bonding Technology	Bonding Temperature	Bonding Pressure	Atmosphere	Bonding Time	Bongding strength	Reference
Cu-Cu	thermo-compression bonding	400℃	25 KN	N2	30 min	4.93 J/m^2	[33]
(111) Cu-Cu	thermo-compression bonding	200℃	0.69 MPa	10^{-3} torr	60 min	4.3 MPa	[42]
HD Cu-HD Cu	thermo-compression bonding	240℃	80 MPa	N2	60 min	-	[44]
nc Cu-nc Cu	thermo-compression bonding	250℃	10 MPa	0.05 Pa	60 min	-	[45]
Cu-Cu	pillar-concave structure	200℃	100 N	air condition	1 min	-	[46]
Cu-Cu	formic acid vapor treatment	240℃	250 MPa	formic acid vapor	5 s	150 MPa	[47]
Cu-Cu	Surface Activated Bonding	RT	1000 Kgf	10^{-8} torr	-	6.47 MPa	[50]
Cu-Cu	Surface Activated Bonding	260℃	0.9 MPa	-	60 min	62.6 MPa	[52]
Cu-Cu	passivation layer	160℃	2.5 Bar	10^{-4} torr	50 min	-	[54]
Cu-Cu	self-assembled monolayer	250℃	2500 mBar	-	60 min	-	[57]
Cu-Cu	wet chemistry pretreatment	180℃	5 MPa	-	3 min	8.98 Mpa	[59]
Cu-Cu	ultrasonic bonding technology	RT	121 N	-	1.5 s	103 Mpa	[60]
Cu-Cu	Cu-Cu indirect bonding	150℃	10 MPa	100 Pa	60 min	15 Mpa	[61]
Cu-Cu	Cu-Cu indirect bonding	250℃	20 MPa	N2	5 min	14.4 Mpa	[62]
SiO_2-SiO_2	wet chemistry pretreatment	400℃	1900 N	10^{-4} mBar	5 min	7.2 Mpa	[68]
SiO_2-SiO_2	plasma surface treatment	200℃	2.5 MPa	10^{-2} Pa	30 min	2.25 J/m^2	[69]

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Table 3 Summary of technical challenges and solutions of different bonding technologies

Bonding Material	Bonding Technology	Bonding mechanism	Technical challenge	solution
Cu-Cu	thermo-compression bonding	increase diffusion rate	high temperature	low temperature bonding
(111) Cu-Cu	thermo-compression bonding	increase diffusion rate	(111) plane Cu preparation	use (111) plane directly
HD Cu-HD Cu	thermo-compression bonding	increase diffusion rate	HD Cu preparation	not suitable for mass production
nc Cu-nc Cu	thermo-compression bonding	increase diffusion rate	nc-Cu preparation	not suitable for mass production
Cu-Cu	pillar-concave structure	increase diffusion rate	pillar and concave preparation; high pressure	not suitable for mass production
Cu-Cu	formic acid vapor treatment	surface treatment	formic acid vapor injection	equipment improvement
Cu-Cu	Surface Activated Bonding	surface treatment	Surface treatment	parameter optimization
Cu-Cu	passivation layer	surface protection	passivation layer preparation	not suitable for mass production
Cu-Cu	self-assembled monolayer	surface protection	monolayer preparation	not suitable for mass production
Cu-Cu	wet chemistry pretreatment	surface treatment	Q-Time control	handle on time
Cu-Cu	ultrasonic bonding technology	surface treatment	surface flatness	equipment improvement

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Cu-Cu	Cu-Cu indirect bonding	surface protection	nanowire preparation	not suitable for mass production
SiO_2-SiO_2	wet chemistry pretreatment	surface treatment	Q-Time control	handle on time
SiO_2-SiO_2	plasma surface treatment	surface treatment	Surface treatment	parameter optimization
Cu-SiO_2	DBI	surface treatment	surface flatness	CMP process optimization
Cu-SiO_2	plasma treatment	surface treatment	surface treatment	parameter optimization

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Table 4 current mainstream hybrid bonding materials

Bonding materials	**Reference**
Au/SiO2	[76-77]
Al/SiO2	[78-79]
Cu/SiO2	[80-81]
Cu/SiO_2/PI	[82-83]
Au/PI	[84]
Cu/PI	[85]
Cu/SiCN	[86-87]

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Table 5. the main solutions of the thermal management

Method	Solution	Reference
Lower power design of the chip	save power consumption as much as possible	[88]
Weaken the hot spot effect of the chip	the heat of the entire chip distribute as evenly as possible	[89]
Structural optimization of heat distribution	optimize the topology and parameters of the heat dissipation path	[90]
Change in microstructure	design the channel only used for heat conduction in the high-power area	[91]
Improve the thermal conductivity of packaging materials	increase the material with high thermal conductivity between the layers; Adopt low thermal resistance material to speed up the internal conduction	[92-93]
Heat dissipation structure	increase external heat dissipation structure such as heat sink	[94-95]
External cooling device:	use strong wind cooling, liquid cooling and other external cooling technology	[96]

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Table 6. the most common reliability threats, potential failures and solutions

Failure mode	Potential failures	Solutions	Reference
Pad to pad dielectric breakdown	Increased pad to pad leakage current, shorts	Optimize voltage ramp stress	[97]
Copper diffusion in the dielectric	Increased leakage current, shorts, dielectric breakdown	Add barrier layer	[98]
Pad to pad misalignment	Increased pad to pad leakage current, dielectric breakdown	Improve alignment accuracy	[99]
Bonding voids	Delamination, opens, decrease of the breakdown voltage	Optimize process parameter	[100]
Electromigration	Voiding resulting in increased contact resistances, or opens	Control voids	[101]